Fully Digital-controlled Power Supply Control IC with Bridgeless PFC and LLC Current-resonant Circuits

MD6751

Data Sheet

Description

The MD6751 is a fully digital-controlled power supply IC, which incorporates a bridgeless PFC control circuit and an LLC current-resonant circuit. The PFC circuit, driven by continuous conduction mode (CCM), is controlled with frequencies suitable for applied input voltages and loads. The LLC circuit incorporates a floating drive circuit that drives an external high-side power MOSFET, in addition to its functionally-rich protections such as capacitive mode detection. These digitally controlled strategies allow application-specific optimal settings. Compared to conventional analog control circuits, the IC can achieve more cost-effective, high-efficient, yet low-noise power systems with fewer external components.

Package

SOP28

Not to scale

Features

- Fully Digital-controlled PFC and LLC Current-resonant Circuits
- Soft Start
- X-capacitor Discharge (No Discharge Resistor Required)
- Bridgeless PFC Circuit
- Continuous Conduction Mode (CCM) PFC Control
- LLC Capacitive Mode Detection
- LLC Automatic Standby Mode
- Protections Include:

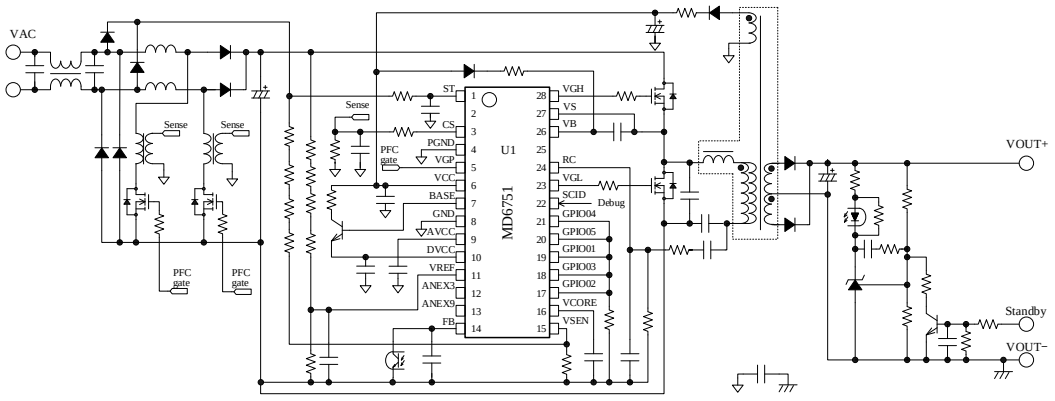
- AC Power Supply Input Undervoltage Lockout
- PFC Output Undervoltage Protection (PFC_UVP)
- PFC Output Overvoltage Protection (PFC_OVP)
- PFC Overcurrent Protection (PFC_OCP)
- LLC High-side Driver Undervoltage Lockout (VB_UVLO)
- LLC Overcurrent Protection (LLC_OCP)
- LLC Overload Protection (LLC_OLP)
- VCC Pin Overvoltage Protection (VCC_OVP)
- Thermal Shutdown (TSD)

Applications

For devices requiring high power supplies such as:

- Audiovisual Equipment (e.g., LCD TV)
- Office Automation Equipment (e.g., Server, Multifunction Printer)
- Industrial Equipment
- Communication Equipment

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). Unless specifically noted, T_A = 25 °C. Surge withstand capability (HBM) of the MD6751 is guaranteed up to 2000 V. Note that the following pins are guaranteed to withstand surges up to 1000 V: 1, 26, 27, 28.

Parameter	Symbol	Pin	Rating	Unit
ST Pin Voltage	V_{ST}	1−8	−0.3 to 600	V
CS Pin Voltage	V_{CS}	3−8	−6.0 to 6.0	V
PGND Pin Voltage	V_{PGND}	4−8	−0.3 to 0.3	V
VGP Pin Voltage	V_{GP}	5−8	−0.3 to V_{CC} + 0.3	V
VCC Pin Voltage	V_{CC}	6–8	−0.3 to 20	V
BASE Pin Voltage	V_{BASE}	7–8	−0.3 to 6.0	V
AVCC Pin Voltage(1)(2)	V_{AVCC}	9–8	−0.3 to 3.6	V
DVCC Pin Voltage(2)	V_{DVCC}	10–8	−0.3 to 3.6	V
VREF Pin Voltage(3)	V_{REF}	11–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
ANEX3 Pin Voltage(3)	V_{ANEX3}	12–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
ANEX9 Pin Voltage(3)	V_{ANEX9}	13–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
FB Pin Voltage	V_{FB}	14–8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
VSEN Pin Voltage	V_{SEN}	15−8	−0.3 to V_{DVCC} + 0.3 and −0.3 to 3.6	V
VCORE Pin Voltage(4)	V_{CORE}	16–8	−0.3 to 2.0(5)	V
GPIO02 Pin Voltage(6)	V_{GPIO02}	17–8	−0.3 to 5.5	V
GPIO02 Pin Current(6)	I_{GPIO02}	17–8	−4.0 to4.0	mA
GPIO03 Pin Voltage(6)	V_{GPIO03}	18–8	−0.3 to 5.5	V
GPIO03 Pin Current(6)	I_{GPIO03}	18–8	−4.0 to 4.0	mA
GPIO01 Pin Voltage(6)	V_{GPIO01}	19–8	−0.3 to 5.5	V
GPIO01 Pin Current(6)	I_{GPIO01}	19–8	−4.0 to 4.0	mA
GPIO05 Pin Voltage(6)	V_{GPIO05}	20–8	−0.3 to 5.5	V
GPIO05 Pin Current(6)	I_{GPIO05}	20–8	−4.0 to 4.0	mA
GPIO04 Pin Voltage(6)	V_{GPIO04}	21–8	−0.3 to 5.5	V
GPIO04 Pin Current(6)	I_{GPIO04}	21–8	−4.0 to 4.0	mA
SCID Pin Voltage	V_{SCID}	22–8	−0.3 to 5.5	V
VGL Pin Voltage	V_{GL}	23–8	−0.3 to V_{CC} + 0.3	V
RC Pin Voltage	V_{RC}	24–8	−6.0 to 6.0	V
VB–VS Pin Voltage	V_{BS}	26–27	−0.3 to 20.0	V
VS Pin Voltage	V_S	27–8	−1 to 600	V
VGH Pin Voltage	V_{GH}	28–8	V_S − 0.3 to V_B + 0.3	V
Operating Ambient Temperature	T_{OP}	—	−40 to 85	°C
Storage Temperature	T_{STG}	—	−40 to 125	°C
Junction Temperature	T_J	—	125	°C

(1) The AVCC pin is the 3.3 V power supply output pin dedicated for the internal LSI chip. Do not apply external voltage to this pin.
(2) Electric potential difference between the AVCC and DVCC pins should be maintained within ±0.3 V （t > 1 ms).
(3) Refers to an analog input pin for 3.3 V systems.
(4) The VCORE pin is the 1.8 V power supply output pin dedicated for digital circuits of the internal LSI chip. Do not apply external voltage to this pin.
(5) Should be rated from −0.3 V to 2.4 V when t < 1 ms (e.g., at startup).
(6) Refers to a digital output pin for 3.3 V systems.

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 17 V.

The check mark in the Chg. column indicates that the item is software-changeable. In addition, the characteristic value in this column is a reference value.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
Startup Circuit, Circuit Current								
Operation Start Voltage	$V_{CC(ON)}$		6–8	13.0	14.0	15.0	V	
Operation Stop Voltage[1]	$V_{CC(OFF)}$		6–8	7.4	8.3	9.2	V	
Startup Current Bias Threshold Voltage[1]	$V_{CC(BIAS)}$		6–8	8.8	9.4	9.9	V	
Circuit Current in Operation	$I_{CC(ON)}$		6–8	—	1.8	4.0	mA	
Circuit Current in Non-operation[2]	$I_{CC(OFF)}$	V_{CC} = 11 V	6–8	—	0.5	1.0	mA	
Startup Current[2]	I_{ST}	V_{ST} = 100 V, V_{CC} = 11 V	1–8	1.8	3.6	6.5	mA	
Maximum Startup Current	$I_{ST(MAX)}$	V_{ST} = 100 V, V_{CC} = 9 V	1–8	2.0	20.0	35.0	mA	
VCC Pin Protection Release Threshold Voltage[1]	$V_{CC(P.OFF)}$		6–8	7.4	8.3	9.2	V	
Circuit Current in Protection Operation	$I_{CC(P)}$	V_{CC} = 10 V	6–8	—	0.5	1.0	mA	
X-capacitor Discharge Delay Time	t_{XCAP}		1–8	30	60	90	ms	
X-capacitor Detection Voltage	ΔV_{XCAP}	10 µs < t < 5 ms [3]	1–8	45	—	—	V	
VCORE Pin Supply Voltage	V_{CORE}		16–8	1.72	1.80	1.88	V	
SCID Pin High Level Detection Voltage[4]	V_{SCID_IH}		22–8	2.0	—	—	V	
SCID Pin Low Level Detection Voltage[4]	V_{SCID_IL}		22–8	—	—	0.8	V	
3.3 V Analog Internal Regulator	V_{AVCC}		9–8	3.233	3.300	3.366	V	
3.3 V Digital Internal Regulator	V_{DVCC}		10–8	3.135	3.300	3.465	V	
External Transistor Drive Voltage for DVCC Pin	V_{BASE}	I_{BASE} = −1 mA	7–8	3.6	—	4.4	V	
VSEN Pin Input UVP Threshold Voltage	$V_{SEN(OFF)}$		15–8	—	0.468	—	V	✓
VSEN Pin Input UVP Release Voltage	$V_{SEN(ON)}$		15–8	—	0.624	—	V	✓
Delay Time of VSEN Pin Input UVP Detection	$t_{VSEN(OFF)}$		15–8	—	10	—	ms	✓
PFC Stage								
CS Pin Offset Voltage[5]	$V_{CS(OFS)}$	V_{CS} = 0 V	3–8	—	0.6	—	V	
PFC Drive Current (Source)	$I_{GP(SRC)}$	V_{CC} = 17 V, V_{GP} = 0 V	5–4	—	−500	—	mA	

[1] $V_{CC\ (OFF)} = V_{CC\ (P.OFF)} < V_{CC\ (BIAS)}$

[2] VCC Pin Supply Current at Startup, $I_{CC(ST)} = I_{ST} - I_{CC(OFF)}$

[3] Detects when the ST pin voltage rises by ΔV_{XCAP} or more in 10 µs < t < 5 ms (see Section 8.6).

[4] Guaranteed by design.

[5] See Figure 2-1.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
PFC Drive Current (Sink)	$I_{GP(SNK)}$	V_{CC} = 17 V, V_{GP} = 17 V	5–4	—	1	—	A	
ANEX3 Pin OCP Threshold Voltage (Low)	$V_{ANEX3(CS\_LO)}$		12–8	—	1.727	—	V	✓
ANEX3 Pin OCP Threshold Voltage (High)	$V_{ANEX3(CS\_HI)}$		12–8	—	0.748	—	V	✓
VREF Pin Threshold Voltage for PFC Output Control	V_{REF}		11–8	—	2.101	—	V	✓
Maximum PFC Oscillation Frequency	f_{MAX_PFC}		5–8	—	199.7	—	kHz	✓
Minimum PFC On-time	$t_{ON(MIN)\_PFC}$		5–8	—	1.07	—	µs	✓
Maximum PFC On-time	$t_{ON(MAX)\_PFC}$		5–8	—	29.9	—	µs	✓
Maximum PFC Off-time	$t_{OFF(MAX)\_PFC}$		5–8	—	21.3	—	µs	✓
VREF Pin PFC_UVP Start Voltage	$V_{REF(UVD)}$		11–8	—	2.021	—	V	✓
VERF Pin PFC_UVP Oscillation Stop Voltage	$V_{REF(UVP)}$		11–8	—	1.103	—	V	✓
VREF Pin PFC_UVP Release Voltage	$V_{REF(UVP\_R)}$		11–8	—	0.552	—	V	✓
PFC_UVP Recovery Delay Time	$t_{(UVP\_R)}$		—	—	819.2	—	ms	✓
VREF Pin PFC_OVP Start Voltage	$V_{REF(OVD)}$		11–8	—	2.151	—	V	✓
VREF Pin PFC_OVP Oscillation Stop Voltage	$V_{REF(OVP)}$		11–8	—	2.233	—	V	✓
VREF Pin PFC_OVP Oscillation Stop Release Voltage	$V_{REF(OVP\_R)}$		11–8	—	2.179	—	V	✓
LLC Stage								
Maximum FB Pin Source Current	$I_{FB(MAX)}$	V_{FB} = 0 V	14–8	−440	−330	−250	µA	
Capacitive Mode Detection Voltage	V_{RC1}		24–8	0.02	0.10	0.18	V	
				−0.18	−0.10	−0.02	V	
RC Pin Threshold Voltage (Fast)	$V_{RC(S)}$		24–8	2.62	2.80	2.98	V	
				−2.98	−2.80	−2.62	V	
RC Pin Offset Voltage[6]	V_{ANEX0}	V_{RC} = 0 V	24–8	—	1.65	—	V	
High-side Driver Operation Start Voltage	$V_{BUV(ON)}$		26–27	5.8	6.8	7.8	V	
High-side Driver Operation Stop Voltage	$V_{BUV(OFF)}$		26–27	5.4	6.4	7.4	V	
LLC Drive Current (Source)	$I_{GL(SRC)}$ $I_{GH(SRC)}$	V_{CC} = 17 V, V_B = 17 V, V_{GL} = 17 V, V_{GH} = 17 V	23–4 28–8	—	–300	—	mA	
LLC Drive Current (Sink)	$I_{GL(SNK)}$ $I_{GH(SNK)}$	V_{CC} = 17 V, V_B = 17 V, V_{GL} = 0 V, V_{GH} = 0 V	23–4 28–8	—	550	—	mA	

[6] See Figure 2-2.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
FB Pin Standby Mode Switching Threshold Voltage	$V_{FB(STB)}$		14–8	—	1.000	—	V	✓
FB Pin Oscillation Stop Voltage in Standby Mode	$V_{FB(OFF)}$		14–8	—	0.413	—	V	✓
FB Pin Oscillation Start Voltage in Standby Mode	$V_{FB(ON)}$		14–8	—	0.516	—	V	✓
VREF Pin LLC Operation Start Voltage	$V_{REF(LLC\_ON)}$		11–8	—	0.552	—	V	✓
VREF Pin LLC Operation Stop Voltage	$V_{REF(LLC\_OFF)}$		11–8	—	0.442	—	V	✓
VREF Pin LLC AC Off Mode Start Voltage	$V_{REF(ACOFF\_ON)}$		11–8	—	1.103	—	V	✓
Lowest LLC Oscillation Frequency in Normal Mode	$f_{MIN\_LLC(NRM)}$		23–4 28–8	—	26.1	—	kHz	✓
Highest LLC Oscillation Frequency in Normal Mode (Maximum)	$f_{MAX\_LLC(NRM\_MAX)}$		23–4 28–8	—	187.5	—	kHz	✓
Minimum LLC Dead Time	$t_{d(MIN)}$		23–4 28–8	—	0.60	—	µs	✓
Maximum LLC Dead Time	$t_{d(MAX)}$		23–4 28–8	—	0.76	—	µs	✓
RC Pin Overcurrent Threshold Voltage (Low)	$V_{RC(L)}$		24–8	—	–1.75	—	V	✓
				—	1.75	—	V	✓
RC Pin OCP Delay Time 1	$t_{RC(OLP)1}$	$V_{RC} \geq V_{RC(L)}$	24− 8	—	153.9	—	ms	✓
RC Pin OCP Delay Time 2	$t_{RC(OLP)2}$	$V_{RC} \geq V_{RC(S)}$	24− 8	—	1.99	—	ms	✓
LLC Standby Mode Delay Time	$t_{FB(STB)}$		14–8	—	512	—	ms	✓
LLC Normal Mode Switching Delay Time	$t_{FB(NRM)}$		14–8	—	3	—	ms	✓
Overvoltage Protection (OVP)								
VCC Pin OVP Threshold Voltage	$V_{CC(OVP)}$		6–8	18.1	19.0	19.7	V	
Digital General-purpose I/O								
GPIO Pin High Level Detection Voltage	V_{IH}		(7)	2.0	—	—	V	
GPIO Pin Low Level Detection Voltage	V_{IL}		(7)	—	—	0.8	V	
Digital Pull-up Resistance	R_{PUP}		(7)	20	60	100	kΩ	
Analog Pull-up Resistance (FB, VSEN)	R_{PUP2}		14–8 15–8	7.9	10.0	12.4	kΩ	
Input Leakage Current	I_L	V_{FBH} = 0 V	8–8	−2	±1	2	µA	
GPIO Pin High Level Output Voltage	V_{OH4}		8–8	2.4	—	—	V	
GPIO Pin Low Level Output Voltage	V_{OL4}		12–8	—	—	0.4	V	

(7) Refers to voltage between the GND pin and all the following pins: GPIO02, GPIO03, GPIO01, GPIO05, GPIO04.

Parameter	Symbol	Conditions	Pin	Min.	Typ.	Max.	Unit	Chg.
Clock Operation								
Internal IRC Oscillation Frequency	f_{IRC}		—	11.64	12.00	12.18	MHz	
Thermal Shutdown (TSD)								
TSD Operating Temperature[8]	$T_{J(TSD)}$		—	125	—	—	°C	
Thermal Characteristics								
Junction-to-Air Thermal Resistance	θ_{J-A}		—	—	—	85	°C/W	

[8] Guaranteed by design.

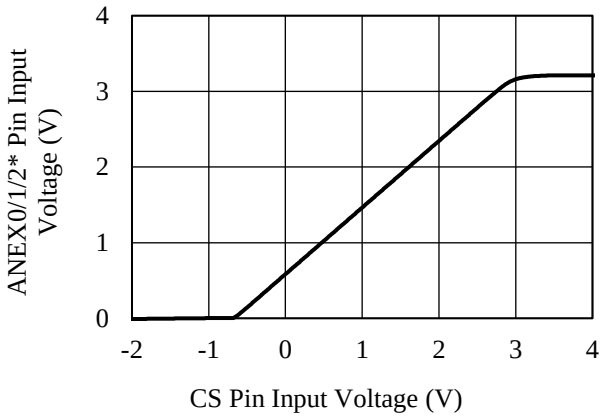


Figure 2-1. CS Pin Offset

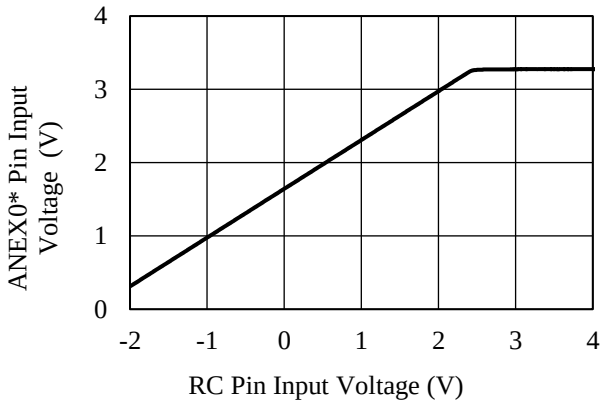
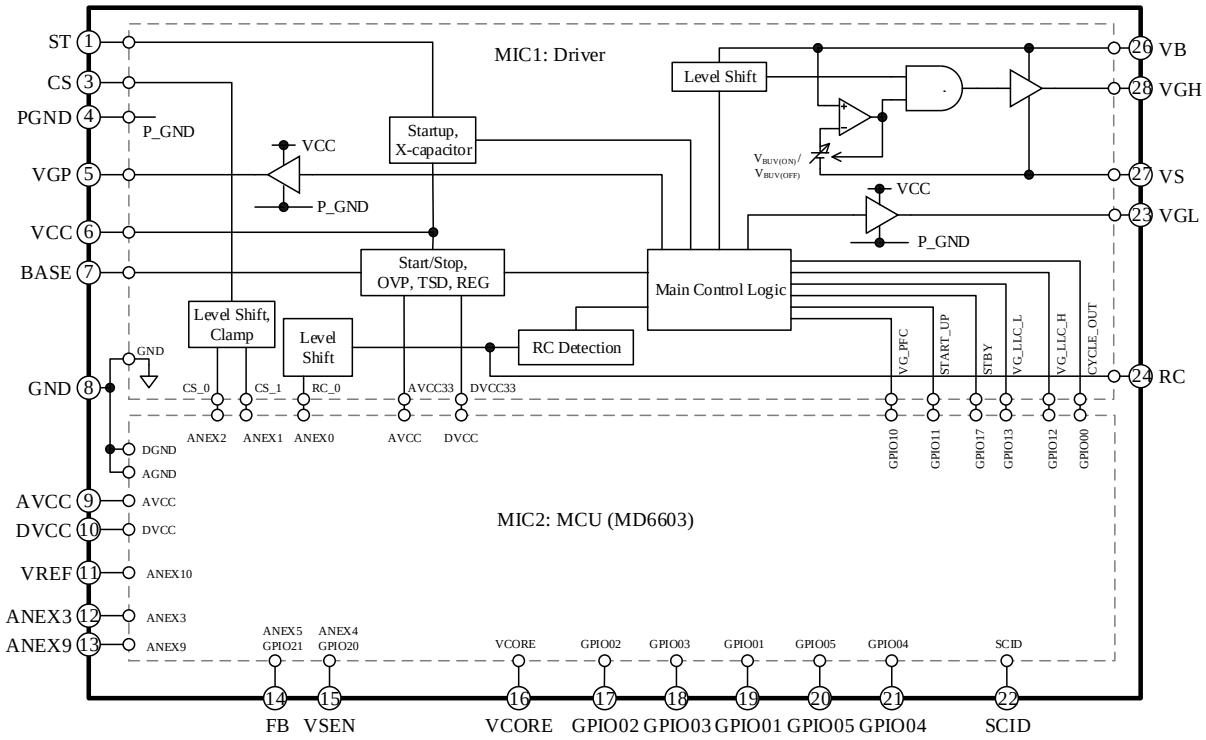


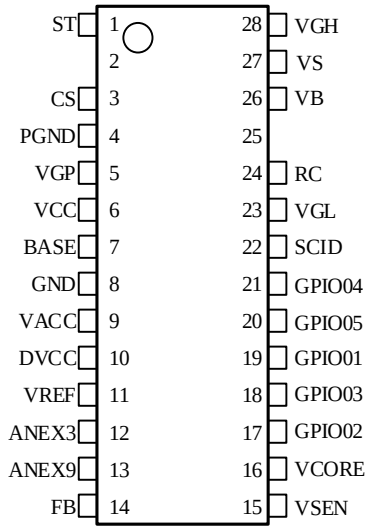
Figure 2-2. RC Pin Offset

* Indicates voltages inside the IC; see the block diagram in Section 3.

3. Block Diagram



4. Pin Configuration Definitions



No.	Name	Description
1	ST	Startup current input; X-capacitor discharge current input
2	—	Pin removed
3	CS	PFC_OCP signal input
4	PGND	Power ground
5	VGP	PFC gate drive output
6	VCC	Logic power supply input; VCC_OVP
7	BASE	External transistor base voltage output for the DVCC pin
8	GND	Ground
9	AVCC	3.3 V analog power supply
10	DVCC	3.3 V digital power supply
11	VREF	PFC constant voltage control signal input
12	ANEX3	Analog input
13	ANEX9	Analog input
14	FB	Power MOSFET control signal input
15	VSEN	Input voltage detection signal input
16	VCORE	Capacitor connection for internal digital circuit supplies
17	GPIO02	General-purpose I/O pin
18	GPIO03	General-purpose I/O pin
19	GPIO01	General-purpose I/O pin
20	GPIO05	General-purpose I/O pin
21	GPIO04	General-purpose I/O pin
22	SCID	Debugging pin (left open if not used)
23	VGL	LLC low-side gate drive output
24	RC	Resonant current detection signal input; LLC_OCP detection signal input
25	—	Pin removed
26	VB	Power supply input for LLC high-side gate drive with UVLO
27	VS	Floating ground of LLC high-side driver
28	VGH	LLC high-side gate drive output

Reference Internal Connection Symbols (MIC1–MIC2; see Section 3)

MIC1 (Driver)	MIC2 (MCU)	Transmission Signal
CYCLE_CUT	GPIO00	LLC capacitive mode detection signal
VG_PFC	GPIO10	PFC PWM signal
START_UP	GPIO11	Startup current control signal
VG_LLC_H	GPIO12	LLC high-side PWM signal
VG_LLC_L	GPIO13	LLC low-side PWM signal
SGND	MODE	Logic ground
STBY	GPIO17	Standby signal
DVCC33	DVCC	3.3 V digital power supply pin
AVCC33	AVCC	3.3 V analog power supply pin
RC_0	ANEX0	Level-shift signal 0 for the RC pin
CS_1	ANEX1	Level-shift signal 1 for the CS pin
CS_0	ANEX2	Level-shift signal 0 for the CS pin

5. Typical Application

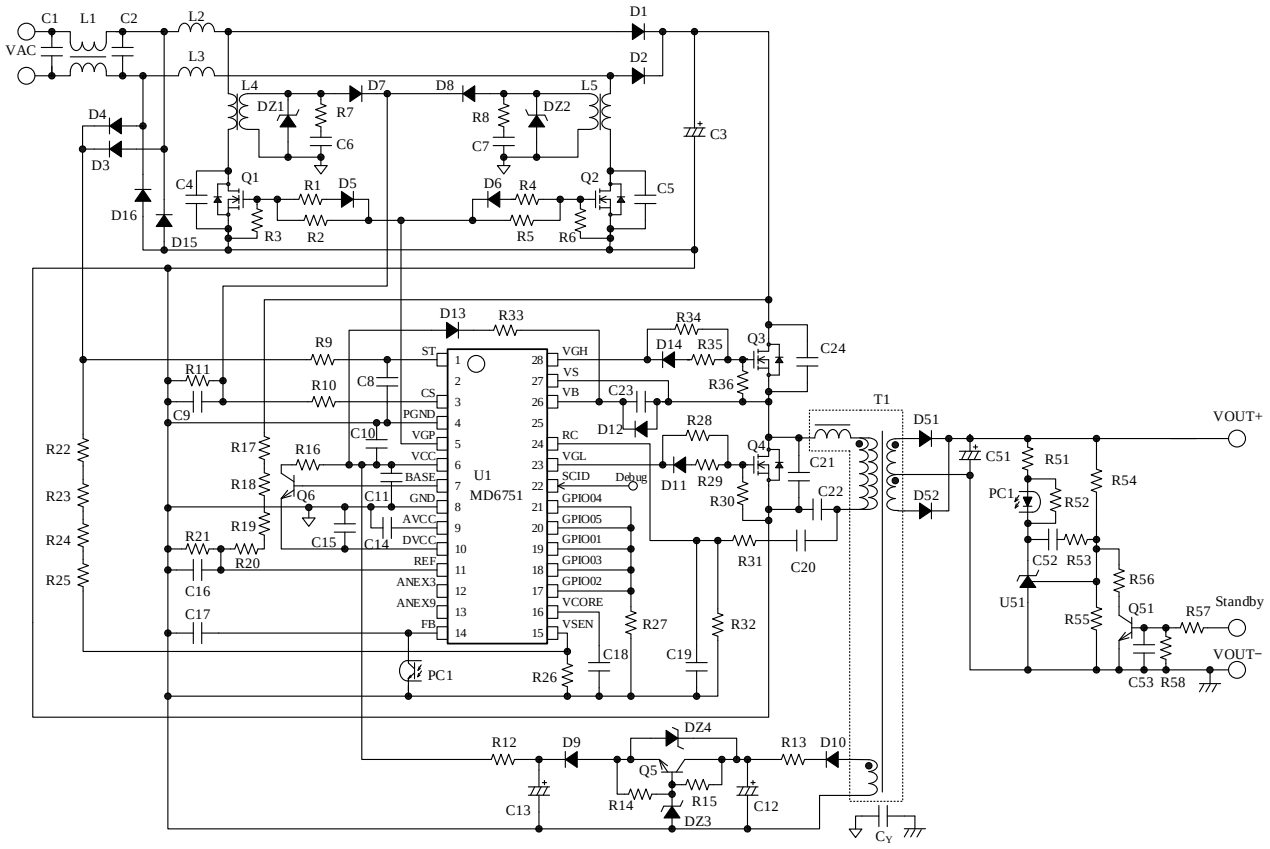


Figure 5-1. Typical Application

6. Physical Dimensions

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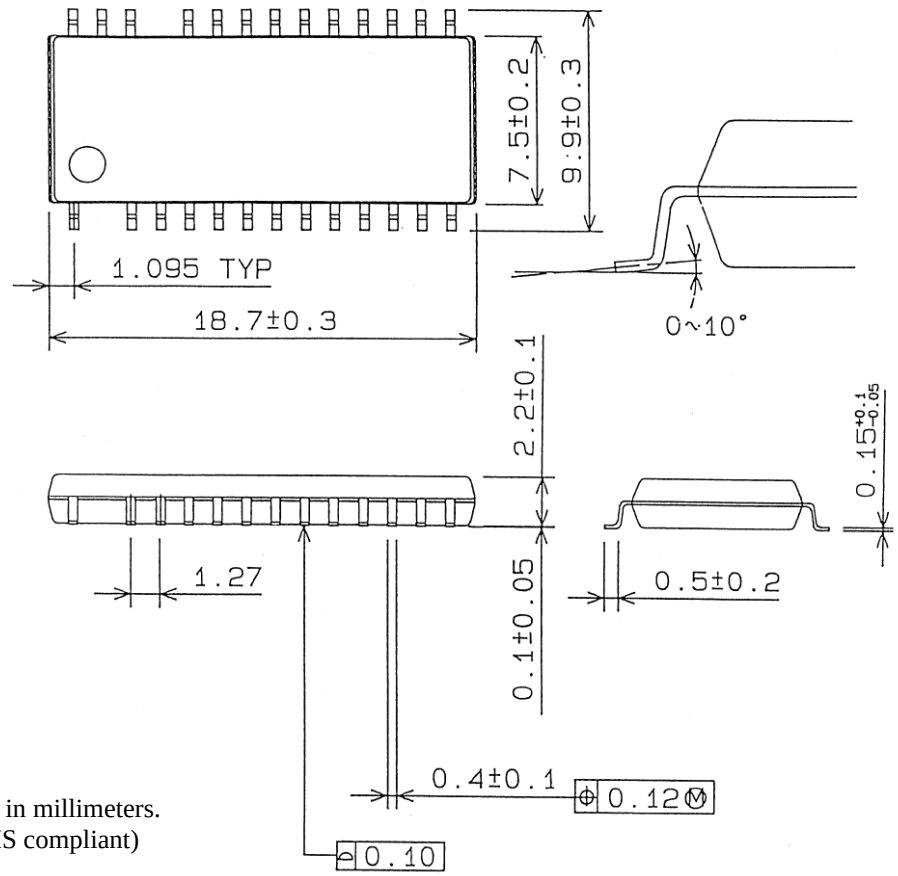
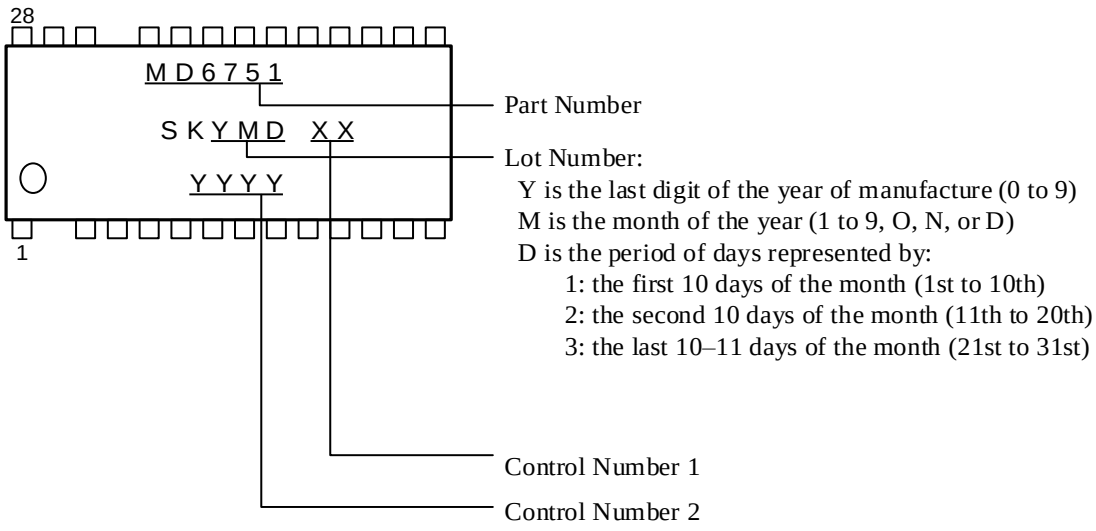


NOTES:
- Dimension is in millimeters.
- Pb-free (RoHS compliant)

7. Marking Diagram



8. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−). For concise descriptions, this section employs notation systems that denote the electrical characteristics symbols listed in Section 2 and the electronic symbol names of the typical application in Section 5.

8.1. General Description

The MD6751 digitally controls a PFC circuit and an LLC current-resonant circuit.

The PFC circuit embedded in the IC requires no input rectifier bridge for its own controlling. The PFC circuit, driven by continuous conduction mode (CCM) in normal operation, is controlled with the frequencies suitable for applied input voltages and loads. By monitoring the output voltage of the PFC circuit with the VREF pin, the IC controls the VGP pin on-time and provides regulated outputs.

The IC has a built-in high-side driver that drives the LLC half-bridge circuit. By monitoring secondary output voltage through an optocoupler, which is connected to the FB pin, the IC controls the oscillation frequencies of the VGH and VGL pins to provide regulated outputs (Section 8.12). In light load operation, the IC automatically switches to standby mode for further enhanced efficiency (Section 8.13). The capacitive mode detection function (Section 8.15) included in the IC requires no setting of minimum oscillation frequencies. Moreover, software-supported dead time setting is available for the MD6751 (Section 8.14).

Protections in the PFC stage include the overcurrent and overload protections (Section 8.9), the overvoltage protection (Section 8.10), and the undervoltage protection (Section 8.11).

Protections in the LLC stage include the high-side driver undervoltage lockout (Section 8.16, and the overcurrent and overload protections (Section 8.17).

In addition to the protections above, the IC also has the following functions: the soft start function (Section 8.4), the bias assist function (Section 8.5), the X-capacitor discharge function for power supply inputs (Section 8.6), the VCC pin overvoltage protection (to prevent secondary outputs from overvoltage; see Section 8.8), and the thermal shutdown (Section 8.18).

8.2. Pin Descriptions

8.2.1. ST

This is the input pin for startup currents and for X-capacitor discharge currents at power supply cutoff. For startup operation, see Section 8.3; for the X-capacitor discharge function, see Section 8.6.

The resistor R9 (about 10 kΩ) is connected to the ST pin. R9 is set at high resistance such that high voltage is applied on it. Therefore, the following must be taken into account in actual designing: select a resistor designed to stand against electromigration; configure R9 with some serial resistors to reduce each applied voltage.

8.2.2. CS

This pin serves as a drain current detector of the power MOSFET in the PFC circuit. In the PFC circuit, which supports high-power applications, current through the power MOSFET is usually detected by the current transformers (L4, L5) as in Figure 8-1. Then, a detection signal is input to the CS pin. Current detection signals transmitted from the CS pin are used for the protections against overcurrent and overload conditions. Section 8.9 provides detailed descriptions on the setting of constants for the CS pin peripheral circuit, the PFC overcurrent protection, and the PFC overload protection.

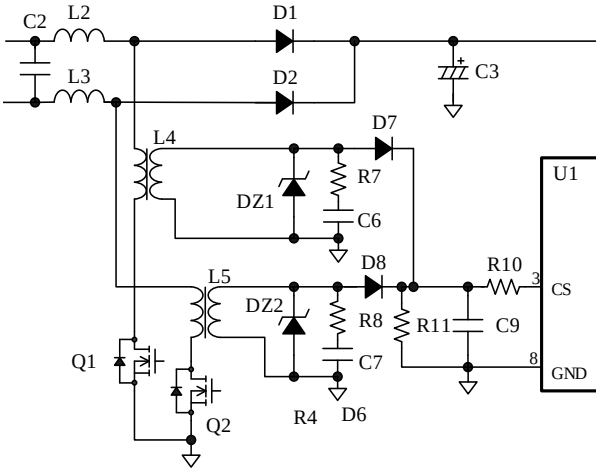


Figure 8-1. CS Pin and Its Peripheral Circuit

8.2.3. GND and PGND

The GND pin is the logic ground pin of the IC; the PGND pin is the power ground pin where driving currents for an external power MOSFET flow through. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, extreme care should be taken when designing a PCB so that currents from the power ground do not affect these pins. For the notes on PCB pattern layouts, see Section 10.

8.2.4. VGP

This is the drive output pin for driving the power MOSFETs (Q1, Q2) in the PFC stage. The pin should be connected to the gates of Q1 and Q2. Respective drive currents are defined as follows: the PFC Drive Current (Source), $I_{GP(SRC)}$ = −500 mA; the PFC Drive Current (Sink), $I_{GP(SNK)}$ = 1 A.

The description hereafter holds up the peripheral circuit of Q1 as an example (but is also applicable to Q2). To increase a rising speed of the gate at power MOSFET turn-off, connect the diode D5 as shown in Figure 8-2. D5, R1, and R2 should be adjusted based on operation performance in an actual application, including a loss in the power MOSFET, gate waveform (a ringing due to pattern layout, etc.), and EMI noise. To prevent malfunction caused by steep dv/dt at power MOSFET turn-off, connect R3, of about 10 kΩ to 100 kΩ, between the gate and source of the power MOSFET with a minimal length of traces.

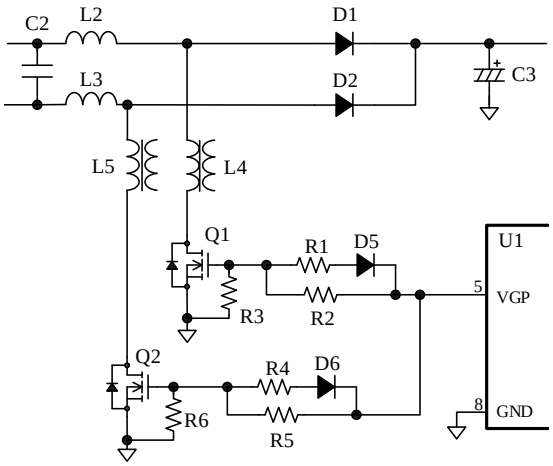


Figure 8-2. VGP Pin and Its Peripheral Circuit

8.2.5. VCC

This is the power supply pin for the built-in control ICs. When the VCC pin voltage increases to $V_{CC(ON)}$ or more, the IC starts operating. When the VCC pin voltage decreases to $V_{CC(OFF)}$ or less, the IC stops operating. This sequence of operations is the VCC Pin undervoltage lockout (VCC_UVLO). In addition to this function, the VCC pin also has the VCC pin overvoltage protection (VCC_OVP). When the VCC pin power is supplied through the auxiliary winding of the LLC transformer, the VCC pin voltage is proportional to the secondary output voltage. Thus, the VCC pin can detect overvoltage conditions in the secondary side.

Section 8.3 describes the startup operation of the IC and the setting of the auxiliary winding; Section 8.8 provides more details on the VCC_OVP. To prevent malfunction induced by supply ripples or other factors, connect 0.01 µF to 0.1 µF ceramic capacitors, C10 and C11, between the VCC and PGND pins, and between the VCC and GND pins, respectively, with a minimal length of traces.

8.2.6. DVCC and BASE

The DVCC pin is the internal 3.3 V digital power supply pin. As Figure 8-3 illustrates, the DVCC pin power is supplied from the auxiliary winding through an external transistor. The BASE pin is connected to the base of this external transistor. To reduce noises on the DVCC pin, connect the capacitor C15 with a capacitance of about 0.1 µF to 1 µF.

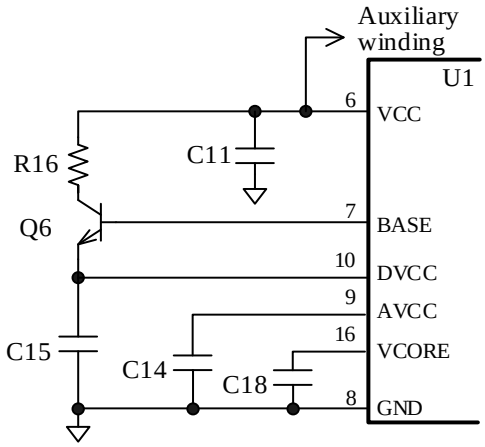


Figure 8-3. Power Stage and Its Peripheral Circuit

8.2.7. AVCC

The AVCC pin is the internal 3.3 V analog power supply pin. The capacitor C14 in Figure 8-3 should have a capacitance of about 0.1 µF to 1 µF. Do not connect anything but C14 to the AVCC pin.

8.2.8. VREF

As shown in Figure 8-4, the output voltage of the PFC stage, $V_{OUT(PFC)}$, divided by the detection resistors is

applied to the VREF pin. Signals input to the VREF pin are used for the constant voltage control in the PFC stage, the overvoltage protection (Section 8.10), and the undervoltage protection (Section 8.11). $V_{OUT(PFC)}$ is determined by the detection resistors, R17 to R21, and can be calculated by the equation below:

$$V_{OUT(PFC)} = \left(\frac{R_{REF1}}{R_{REF2}} + 1\right) \times V_{REF} . \quad (1)$$

Where:

V_{REF} is the VREF pin threshold voltage (2.101 V),
R_{REF1} is the combined resistance of the resistors R17 to R20, and
R_{REF2} is the resistance of R21 (≈ 33 kΩ).

The resistors of R_{REF1} are set at high resistance such that high voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; configure R_{REF1} with some serial resistors to reduce each applied voltage.

To reduce switching noises, connect the capacitor C16 with a capacitance of about 1000 pF, as near as possible to the VREF pin.

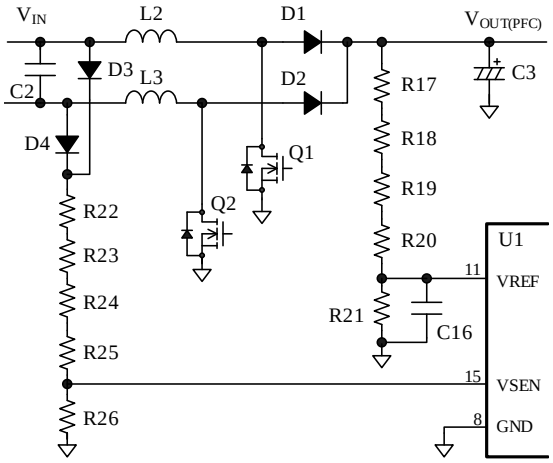


Figure 8-4. VREF and VSEN Pins and Their Peripheral Circuit

8.2.9. ANEX3 and ANEX9

These are the input pins for analog signals. The ANEX3 pin is internally connected to the comparator and the AD converter, whereas the ANEX9 pin is internally connected to the AD converter. Leave these pins open if not used.

For more details, refer to MD6603 data sheet.

8.2.10. FB

This pin is used for controlling constant voltages in the LLC stage. As Figure 8-5 shows, the optocoupler PC1 and the capacitor C17 should be connected to the FB pin. The FB pin controls the on-times of the high- and low-side power MOSFETs (duty cycle = 50%). When the FB pin voltage decreases to $V_{FB(STB)}$ = 1.000 V or less along with a lowering in the secondary output voltage, the IC automatically switches to standby mode.

Section 8.12 provides more details on the constant voltage control; Section 8.13 describes the standby mode function and the settings of the FB pin and its peripheral circuit.

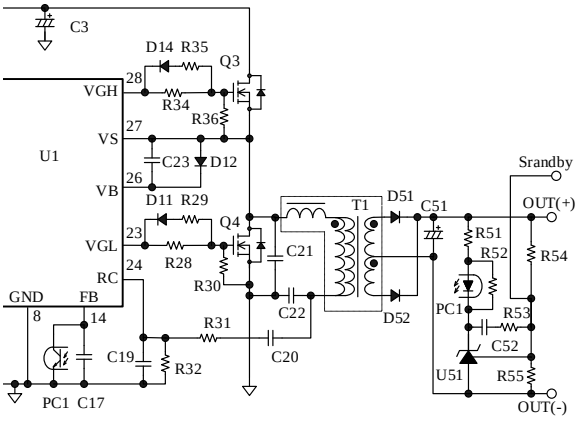


Figure 8-5. LLC Circuit

8.2.11. VSEN

As shown in Figure 8-4, the input voltage, V_{IN}, divided by the detection resistors is applied to the VSEN pin. Signals input to the VSEN pin are used for the undervoltage lockout and the input voltage off-state detection. For more detailed functional descriptions and the peripheral constants of the VSEN pin, see Section 8.7.

8.2.12. VCORE

The VCORE pin is the internal 1.80 V power supply pin. The capacitor C18 should have a capacitance of 0.1 µF. Do not connect anything but C18 to the VCORE pin.

8.2.13. GPIO01 to GPIO05

These pins are the general-purpose I/O pins. For more details, refer to MD6603 data sheet.

These pins must be all connected to the GND pin if not used.

8.2.14. SCID

This is the debugging pin. For detailed functional descriptions, such as software debugging, and software programming (erasing and writing) to the programs on the flash memory, refer to MD6603 data sheet.

Leave this pin open if not used.

8.2.15. RC

This pin operates as the capacitive mode detector. The capacitor C20 and the resistor R32 should be connected to the RC pin, as in Figure 8-5. Signals input to the RC pin is used for detecting the conditions such as a capacitive mode operation or an overcurrent state in the LLC stage. Section 8.15 explains the capacitive mode detection function and the settings of the RC pin and its peripheral circuit; Section 8.17 gives a detailed explanation on the LLC overcurrent protection.

8.2.16. VGL and VGH

These pins are the drive output pins for driving the power MOSFETs in the LLC stage. The VGL pin acts as a low-side driver, whereas the VGH pin acts as a high-side driver. Respective drive currents are defined as follows: the LLC Drive Current (Source), $I_{GL(SRC)} = I_{GH(SRC)} = -300$ mA; the LLC Drive Current (Sink), $I_{GL(SNK)} = I_{GH(SNK)} = 550$ mA.

The description hereafter holds up the peripheral circuit of Q4 as an example (but is also applicable to Q3). To increase a falling speed of the gate at power MOSFET turn-off, connect the diode D11 as shown in Figure 8-5. R28, R29, and D11 should be adjusted based on operation performance in an actual application, including a loss in the power MOSFET, gate waveform (a ringing due to pattern layout, etc.), and EMI noise. To prevent malfunction caused by steep dv/dt at power MOSFET turn-off, connect R30, of about 10 kΩ to 100 kΩ, between the gate and source of the power MOSFET with a minimal length of traces. When adjusting gate resistances, note that gate waveforms of the power MOSFETs must be checked whether a proper amount of dead time is ensured based on the reference waveforms depicted in Figure 8-6.

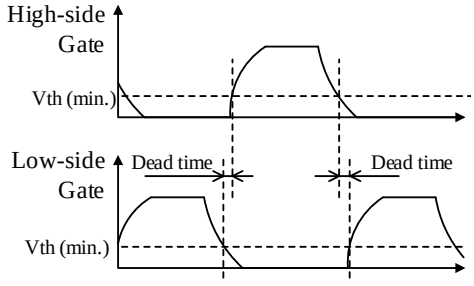


Figure 8-6. Dead Time Confirmation

8.2.17. VB and VS

The VB pin is the input of the high-side floating power supply, whereas the VS pin is the ground of the high-side floating power supply. The MD6751 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins (see Section 8.16).

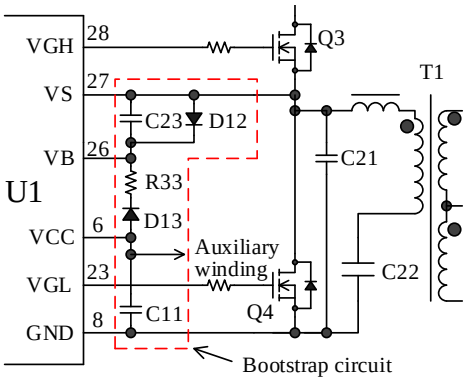


Figure 8-7. Bootstrap Circuit

Figure 8-7 is a schematic diagram of the bootstrap circuit that drives the high-side power MOSFET (Q3). In the condition where the high-side power MOSFET is turned off and the low-side power MOSFET (Q4) is turned on, the VS pin voltage has almost the same potential as the ground. Then, C23 is charged with the VCC pin. When the voltage between the VB and VS pins (hereafter "VB–VS voltage") increases to $V_{BUV(ON)} = 6.8$ V or more, the internal high-side driver starts operating. When VB–VS voltage decreases to $V_{BUV(OFF)} = 6.4$ V or less, the internal high-side driver stops operating (i.e., VB_UVLO). The VB_UVLO protects the IC in case both ends of C23 and D12 are shorted. The bootstrap circuit components must meet the following:

- **D13**

D13 should be a fast recovery diode with a short recovery time and a low reverse current. When the maximum supply input voltage is specified at 265 AVC, it is recommended to use a fast recovery diode with $V_{RM} = 600$ V.

- **C11, C23, R33**

The values of C11, C23, and R33 are determined by the following parameters: the total amount of gate charges of the external power MOSFETs, Qg; the amount of a voltage dip between the VB and VS pins during operation at the lowest oscillation frequency. C11, C23, and R33 should be adjusted according to voltages measured by a high-voltage differential probe so that VB–VS voltage exceeds $V_{BUV(ON)} = 6.8$ V. C11 and C23 should be film or ceramic capacitors with a low ESR and

a low leakage current. The reference value of C11 is 0.47μF to 1 μF. The time constants of C23 and R33 should be set within 500 ns. C23 should have a capacitance of 0.047 μF to 0.1 μF; R33 should have a resistance of 2.2 Ω to 10 Ω.

- **D12**

D12 is used for protecting the VS pin from having a negative potential. D12 should be a Schottky diode with a low forward voltage so that VB–VS voltage does not fall below −0.3 V of its absolute maximum rating.

8.3. Startup Operation

The MD6751 incorporates its own startup circuit, which is connected to the ST pin. When the ST pin voltage rises, the constant startup current regulated inside the IC (I_{ST} = 3.6 mA) starts charging the electrolytic capacitor C13, which is connected to the VCC pin. When the VCC pin voltage increases to $V_{CC(ON)}$ = 14.0 V in the state where $V_{REF(LLC\_ON)}$ = 0.552 V or more, the VGH and VGL pins in the LLC stage start oscillating in standby mode (see Section 8.13). Then, the secondary output voltage starts rising.

Subsequently, when the FB pin voltage increases to $V_{FB(STB)}$ = 1.000 V or more and remains in this condition for $t_{FB(NRM)}$ = 3 ms or longer, the VGP pin in the PFC stage starts oscillating.

t_{START} is a period of time until an internal control circuit starts operating (see Figure 8-9), and is determined by the capacitance of C13. The approximate startup time, t_{START}, can be calculated by Equation (2) below:

$$t_{START} = C13 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{I_{ST} - I_{CC(OFF)}}. \quad (2)$$

Where:

t_{START} is the startup time of the IC,
$V_{CC(INT)}$ is the initial VCC pin voltage (V),
I_{ST} is the startup current (3.6 mA), and
$I_{CC(OFF)}$ is the circuit current in non-operation (0.5 mA).

After the IC starts switching operation, a voltage to be applied on the VCC pin is the rectified auxiliary winding voltage, V_D, as shown in Figure 8-8. After the power startup sequence ends, the startup circuit turns off automatically to eliminate the power dissipation by itself.

The winding turns of the auxiliary winding D should be adjusted so that the VCC pin voltage falls within the range defined by Equation (3), in accordance with the power supply specifications giving the variation range of input and output voltages. The reference voltage across an auxiliary winding is about 17 V.

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.3 V or less, the IC stops operating.

The range of the VCC pin voltage is:

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.}),$$

that is,

$$9.9\ \text{V} < V_{CC} < 18.1\ \text{V}. \quad (3)$$

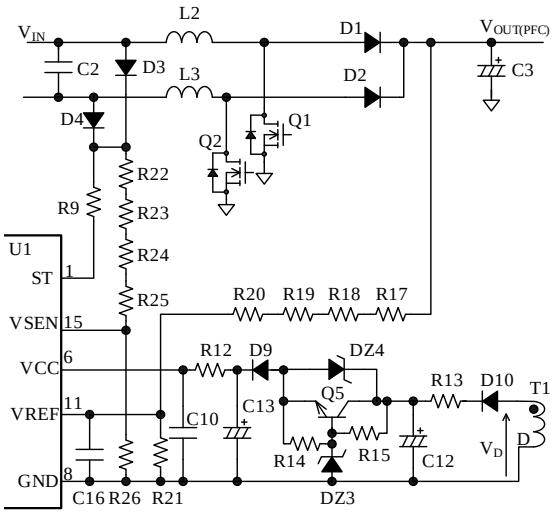


Figure 8-8. VCC Pin and Its Peripheral Circuit

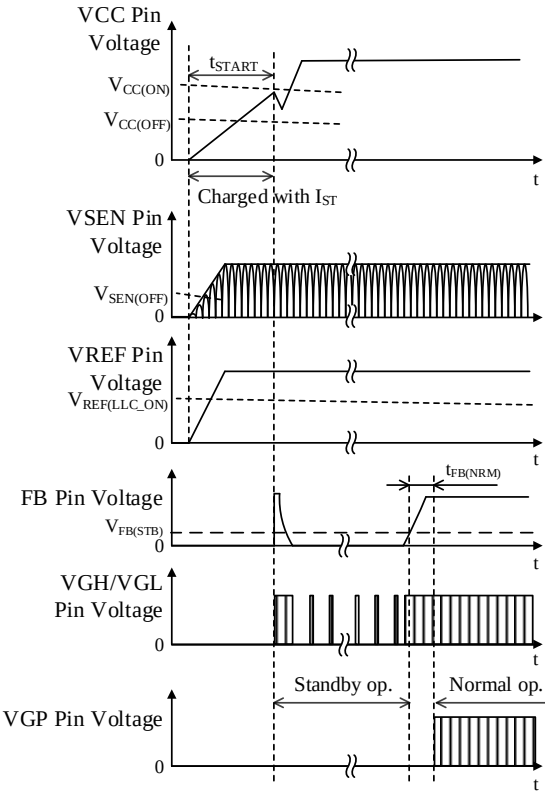


Figure 8-9. Operational Waveforms at Startup

8.4. Soft Start Function

Figure 8-10 shows operational waveforms of the soft start operation at startup. The IC has the soft start function to reduce stresses on the peripheral components, and to prevent the LLC circuit from operating in capacitive mode operation. During the soft start operation, output power increases as the switching frequencies of the VGH and VGL pins gradually decrease. After the output power increases, the IC operates with oscillation frequency control using feedback signal.

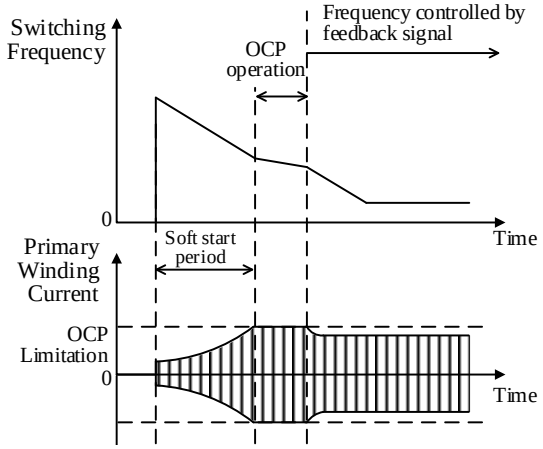


Figure 8-10. Soft Start Operation

8.5. Bias Assist Function

The IC has the bias assist function to suppress a voltage drop in the VCC pin voltage. When the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.4 V, even during normal operation, the bias assist function is activated. When the bias assist function is activated, the startup current, $I_{ST(MAX)}$ = 20.0 mA, is supplied to the VCC pin through the startup circuit. As a result, the VCC pin voltage drop can be suppressed.

8.6. X-capacitor Discharge Function

Generally, a line filter is inserted in the input side of a switching power supply, as illustrated in Figure 8-11.

The voltage across the capacitor of the line filter (i.e., X-capacitor, C_X) must be decreased to 37% or less of a peak AC input voltage within 1 second after AC input voltage cutoff (as per IEC60950 safety requirements). Therefore, the discharge resistor, R_{DIS}, is connected in parallel with C_X, as a common approach to meet the requirements. While the AC input voltage is applied, R_{DIS} constantly consumes power. Power dissipation in R_{DIS}, P_{RDIS}, can be obtained by Equation (4), below:

$$P_{RDIS} = \frac{V_{AC(RMS)}{}^2}{R_{DIS}}. \quad (4)$$

Let $V_{AC(RMS)}$ be the effective value of the AC input voltage. Hence, if the combined resistance of R_{DIS} = 3 MΩ and the AC input voltage = 265 V, P_{RDIS} becomes 23 mW.

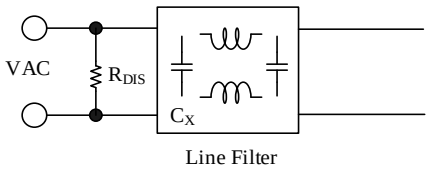


Figure 8-11. Typical Line Filter Circuit

To improve circuit efficiency, the MD6751 has the X-capacitor discharge function instead of implementing such commonly used R_{DIS}.

As Figure 8-12 shows, D3, D4, and R9 are connected to the ST pin, through the traces leading from the AC input line.

When the ST pin voltage rises by ΔV_{XCAP} = 45 V or more in a certain period, the IC determines that AC is input.

When the X-capacitor Discharge Delay Time, t_{XCAP} = 60 ms or longer, elapses after a cutoff state of the AC input voltage, the X-capacitor is discharged by a constant current, I_{ST} = 3.6 mA (see Figure 8-13).

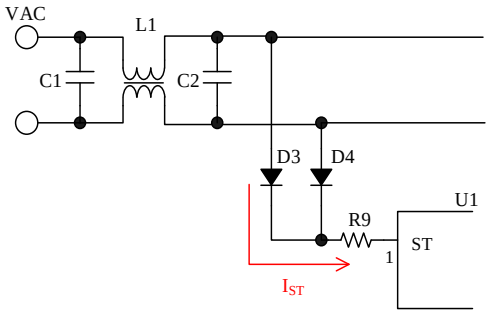


Figure 8-12. ST Pin and Its Peripheral Circuit

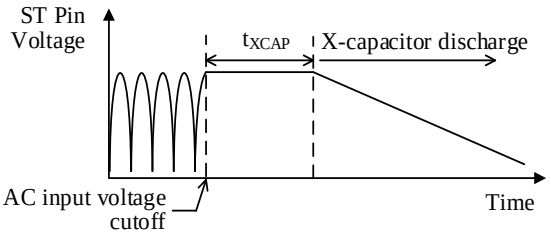


Figure 8-13. Operational Waveform at X-capacitor Discharge

8.7. AC Power Supply Input Undervoltage Lockout

The IC incorporates the AC power supply input undervoltage lockout. This function allows the IC to stop the switching operation of the VGP pin when a low AC line input voltage is detected, thus preventing from excessive input current and overheating.

As depicted in Figure 8-14, the VSEN pin monitors the AC input voltage. When the AC input voltage falls below its normal-state level and $V_{SEN} \leq V_{SEN(OFF)}$ of 0.468 V; or when VSEN stays unvaried, the IC stops the VGP pin switching operation after a lapse of $t_{VSEN(OFF)}$ = 10 ms. During the function operation, the IC controls the LLC circuit with "AC off mode".

When all the following conditions are met, the VGP pin resumes switching operation according to output load and the LLC circuit returns to normal operation: the AC input voltage is rising, the IC is in operation, and $V_{SEN} \geq V_{SEN(ON)}$ of 0.624 V.

The reference resistance of R26, the resistor to be connected to the VSEN pin, is about 20 kΩ. R22 to R26 should be selected based on operation performance in an actual application. R22 to R25 are set at high resistance such that high voltage is applied on them. Therefore, the following must be taken into account in actual designing: select resistors designed to stand against electromigration; connect these resistors in series to reduce each applied voltage.

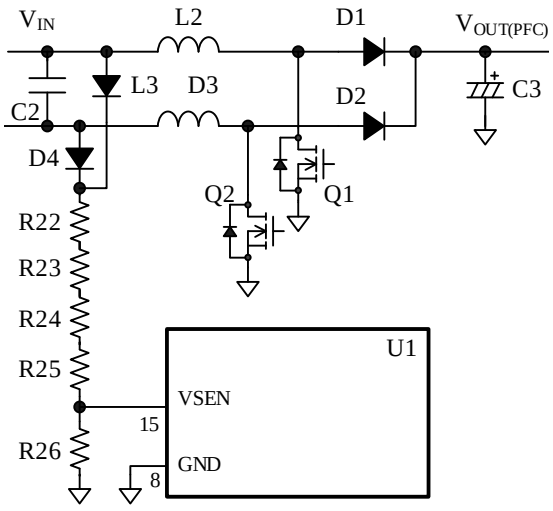


Figure 8-14. VSEN Pin and Its Peripheral Circuit

8.8. VCC Pin Overvoltage Protection

When the voltage between the VCC and GND pins increases to $V_{CC(OVP)}$ = 19.0 V or more, the VCC pin overvoltage protection (VCC_OVP) is activated. Then, the IC stops switching operation.

During the VCC_OVP operation, the circuit current decreases to $I_{CC(P)}$ = 0.5 mA, and the bias assist function is disabled. When the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.3 V or less after the function disablement, the IC releases the VCC_OVP operation and restarts. Then, the VCC pin voltage is increased by startup current, and reaches $V_{CC(ON)}$, allowing the IC to resume switching operation. In this way, the intermittent operation by the VCC_UVLO is repeated during the VCC_OVP operation.

When the VCC pin voltage is supplied through the auxiliary winding of the transformer, the VCC pin voltage is proportional to the output voltage. As a result, the VCC pin can detect a secondary overvoltage condition caused by abnormality (e.g., when an output voltage detection circuit is open).

The approximate value of the secondary output voltage, $V_{OUT(OVP)}$, at the VCC_OVP activation can be calculated by Equation (5) below:

$$V_{OUT(OVP)} = \frac{V_{OUT(NRM)}}{V_{CC(NRM)}} \times 19.0\ (V)\ . \quad (5)$$

Where $V_{OUT(NRM)}$ is the output voltage in normal operation, and $V_{CC(NRM)}$ is the VCC pin voltage in normal operation.

8.9. PFC Overcurrent Protection

The MD6751 has the PFC overcurrent protection (PFC_OCP). This function monitors the CS pin voltage to detect a peak drain current of the power MOSFET on a pulse-by-pulse basis, and limits the on-time of the VGP pin when the CS pin voltage reaches the PFC_OCP threshold voltage. The PFC_OCP threshold voltage can be set by the ANEX3 pin, with a range of $V_{ANEX3(CS\_LO)}$ to $V_{ANEX3(CS\_HI)}$.

In all AC input voltage specifications, the current transformer should be set so that CS pin voltage stays within the range of $V_{ANEX3(CS\_LO)}$ to $V_{ANEX3(CS\_HI)}$. The winding turns ratio of the current transformer, n, is calculated as follows:

$$n = \frac{I_{D(PEAK)}}{V_{OCP}} \times R_{CS}\ . \quad (6)$$

Where:

$I_{D(PEAK)}$ is the drain current in the PFC_OCP operation,

R_{CS} is the current detection resistance of the current transformer (i.e., R11 in Figure 5-1), and

V_{OCP} is the PFC_OCP threshold voltage (i.e., $V_{ANEX3(CS\_HI)}$).

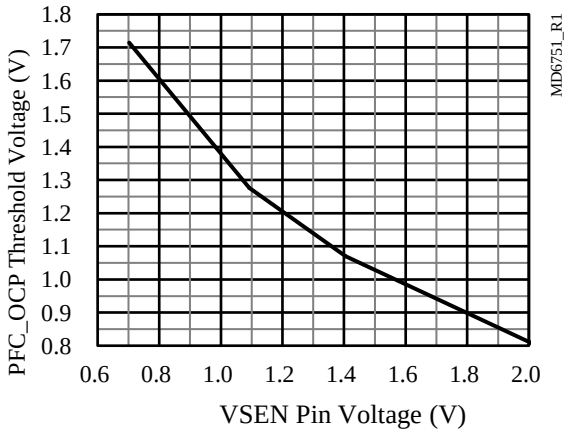


Figure 8-15. PFC_OCP Threshold Voltage vs. VSEN Pin Voltage (Peak)

8.10. PFC Overvoltage Protection

The VREF pin detects an overvoltage condition of the PFC output. Figure 8-16 depicts operational waveforms of the PFC overvoltage protection (PFC_OVP). When the VREF pin voltage increases to $V_{REF(OVD)}$ = 2.151 V or more, the on-time of the VGP pin is limited. Besides, when the VREF pin voltage still increases to $V_{REF(OVP)}$ = 2.233 V or more, the PFC_OVP is activated to stop the VGP pin oscillation and to avoid a further increase in the output voltage. When the VREF pin voltage decreases to $V_{REF(OVP\_R)}$ = 2.179 V or less along with a lowering in the output voltage, the VGP pin resumes oscillating. In this way, the intermittent operation is repeated while the overvoltage condition persists. When the causes of the overvoltage condition are eliminated, the IC automatically returns to normal operation. During the PFC_OVP operation, the VGH and VGL pins in the LLC circuit continue their switching operations.

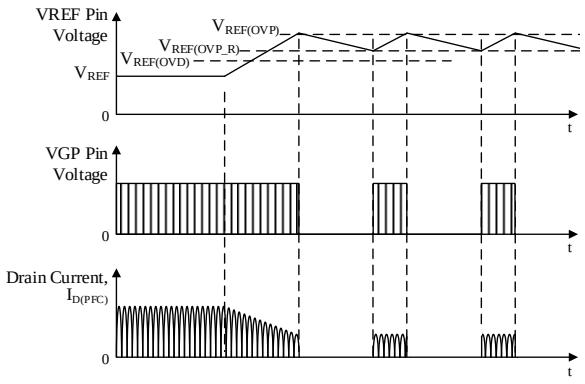


Figure 8-16. PFC_OVP Operational Waveforms

8.11. PFC Undervoltage Protection

The VREF pin also detects an undervoltage condition of the PFC output. Figure 8-17 depicts operational waveforms of the PFC undervoltage protection (PFC_UVP). When the VREF pin voltage decreases to $V_{REF(UVD)}$ = 2.021 V or less, the on-time of the VGP pin is lengthened. Besides, when the VREF pin voltage still decreases $V_{REF(UVP)}$ = 1.103 V or less, the PFC_UVP is activated to stop the VGP pin oscillation. When the VREF pin voltage decreases even further to $V_{REF(UVP\_R)}$ = 0.552 V or less after that, the VGP pin resumes oscillating. During the non-oscillating period of the VGP pin, if the VREF pin voltage does not go below $V_{REF(UVP\_R)}$ within $t_{(UVP\_R)}$ = 819.2 ms, the VGP pin resumes oscillating at the time that $t_{(UVP\_R)}$ elapses. In this way, the intermittent operation is repeated while the output undervoltage condition persists. When the causes of the undervoltage condition are eliminated, the IC automatically returns to normal operation.

During the PFC_UVP operation, the VGH and VGL pins in the LLC circuit continue their switching operations.

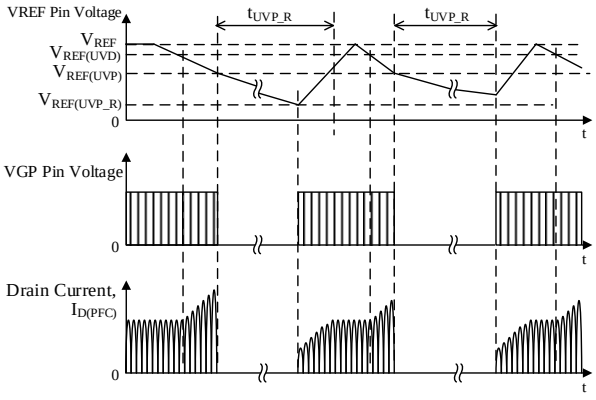


Figure 8-17. PFC_UVP Operational Waveforms

8.12. LLC Constant Voltage Control

Figure 8-18 is a schematic diagram of the FB pin and its peripheral circuit. The capacitor C19 and the optocoupler PC1 are connected to the FB pin. The switching frequencies of the VGH and VGL pins are determined by the system where the optocoupler PC1 controls the feedback source current from the FB pin. In light load operation, the FB pin voltage decreases as the feedback source current increases. The IC reduces the on-times of the VGH and VGL pins, and raises their oscillation frequencies. Conversely, the FB pin voltage increases in heavy load operation. The IC extends the on-times of the VGH and VGL pins, and lowers their oscillation frequencies. By regulating oscillation frequencies in this manner, the IC can stabilize an output voltage (controlled in an inductance area).

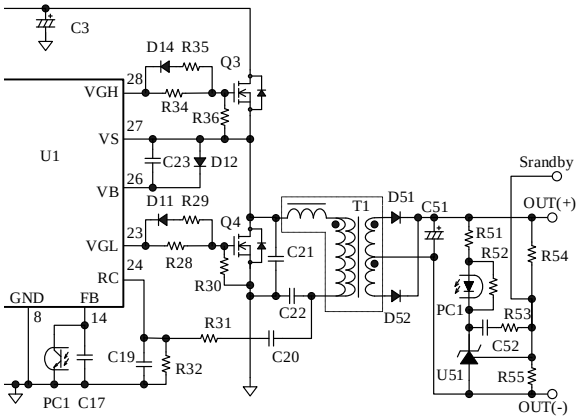


Figure 8-18. FB Pin and Its Peripheral Circuit

Figure 8-19 shows how the oscillation frequencies of the VGL and VGL pins change according to the FB pin voltage. The secondary error amplifier should be designed so that collector current passing through the optocoupler PC1 is higher than 330 µA that is the absolute maximum source current of the FB pin. In particular, the current transfer ratio, CTR, of the optocoupler must take its performance decline over time into account in actual designing. C17 should have a capacitance of about 1000 pF.

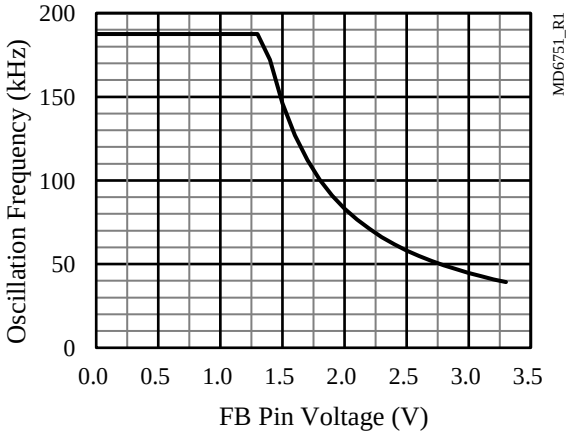


Figure 8-19. VGH/VGL Pin Oscillation Frequency vs. FB Pin Voltage

8.13. LLC Automatic Standby Mode Function

The IC is equipped with the automatic standby mode function which increases efficiency in its light load operation. Figure 8-21 shows operational waveforms in standby mode.

When the state where the secondary output voltage decreases and the FB pin voltage keeps $\leq V_{FB(STB)}$ of 1.000 V for $t_{FB(STB)}$ = 512 ms or longer, the IC automatically transits to standby mode. In standby mode, the VGP pin stops oscillating, whereas the VGH and VGL pins operate with burst oscillation.

Subsequently, when the FB pin voltage increases to $V_{FB(STB)}$ or more and remains in this condition for $t_{FB(NRM)}$ = 3 ms or longer, the VGP pin resumes oscillating. Then, the IC returns to normal operation.

Taking Figure 8-20 as an example, when the Standby input pin becomes logic low, the secondary output voltage decreases. Then, the IC transits to standby mode.

The burst oscillation, which repeats oscillating and non-oscillating periods, reduces switching losses. Generally, a burst oscillation frequency is set at several hertz to improve efficiency in light load operation. Moreover, the IC has the soft turn-on/off function to prevent drain currents from varying steeply in burst oscillation mode, thus suppressing audible noise in the transformer.

The oscillating and non-oscillating periods in burst oscillation operation depend on the FB pin voltage. When the FB pin voltage decreases to $V_{FB(OFF)}$ = 0.413 V or lower, the VGH and VGL pins increase their oscillation frequencies to lower switching currents gradually, and then stop oscillation (i.e., non-oscillating period). When the FB pin voltage increases to $V_{FB(ON)}$ = 0.516 V or more, the VGH and VGL pins start oscillating and decrease their oscillation frequencies to raise switching currents gradually.

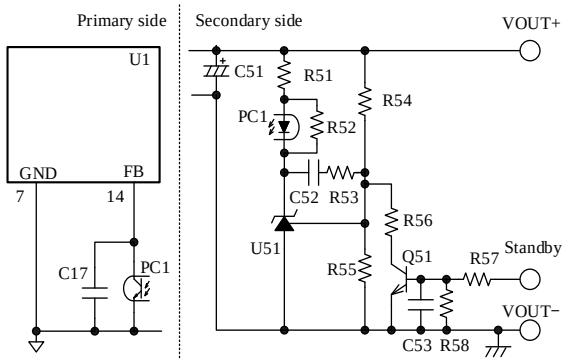


Figure 8-20. Standby Signal Input Circuit

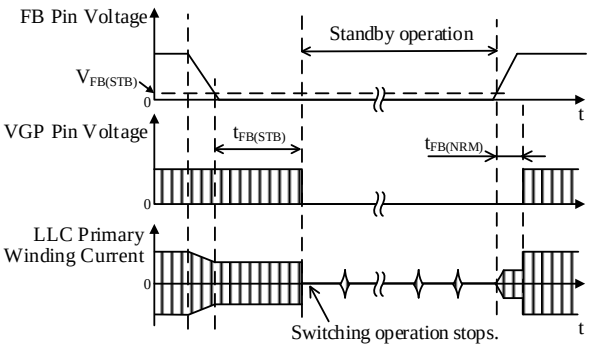


Figure 8-21. Operational Waveforms in Standby Mode

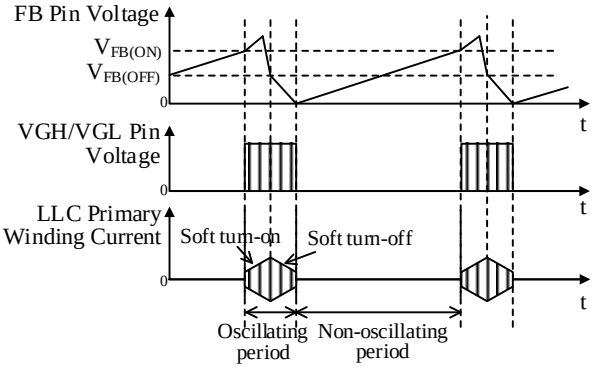


Figure 8-22. Operational Waveforms in Burst Oscillation Mode

8.14. LLC Dead Time

A dead time is a period of time when both of the high- and low-side power MOSFETs in the LLC stage turn off. When the dead time is shorter than a voltage resonance period as in Figure 8-23, the power MOSFETs turn on or off during the voltage resonance period. In such case, switching loss increases due to hard switching of the power MOSFETs.

Be sure to set a dead time so that it falls within the range, from $t_{d(MIN)}$ = 0.60 µs to $t_{d(MAX)}$ = 0.76 µs, for which the power supply operates within all the allowable operating ranges and avoids the zero voltage switching (ZVS) failure shown in Figure 8-23.

Figure 8-25 depicts how a dead time varies according to the FB pin voltage. Also, actual operations must be checked to ensure that power MOSFETs operate with the zero current switching (ZCS) under the following conditions (i.e., check if a period in which drain current flows through a body diode exists for about 600 ns, as in Figure 8-24):

- When an output power is minimum in a maximum input voltage specification
- When an output power is maximum in a minimum input voltage specification

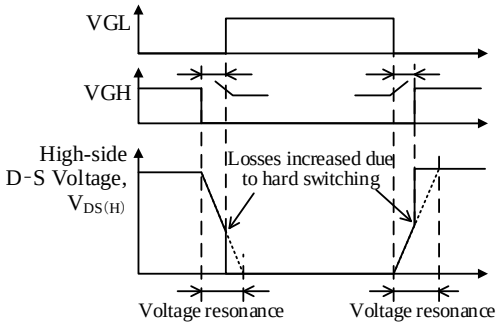


Figure 8-23. Waveforms When ZVS Failure Occurs

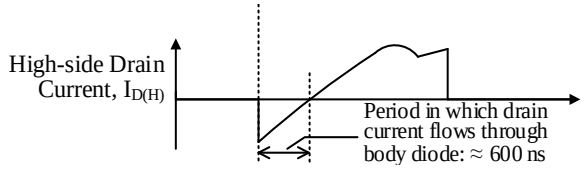


Figure 8-24. Point to Be Checked in ZCS

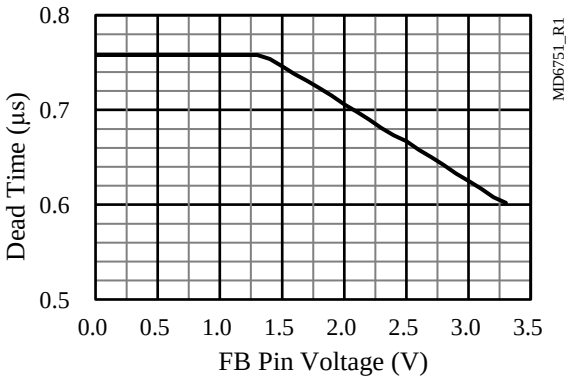


Figure 8-25. Dead Time vs. FB Pin Voltage

8.15. LLC Capacitive Mode Detection Function

The current resonant power supply must operate in the inductive area shown in Figure 8-26. In the capacitive area, the power supply enters capacitive mode. To prevent such operation, it is generally required to set a minimum oscillation frequency higher than f_0 defined for each power supply specification.

The IC has the capacitive mode detection function that constantly maintains its frequency higher than f_0, thereby requiring no setting of minimum oscillation frequencies. Accordingly, enhanced design-friendliness will be added to your application. In addition, using switching frequency of near f_0 increases the transformer use efficiency.

The RC pin detects a resonant current to judge a capacitive operation. When the IC detects the capacitive operation for the OLP delay time, $t_{RC(OLP)1}$ or $t_{RC(OLP)2}$, or longer, the overload protection (OLP) is activated to stop the oscillation operations of the VGH, VGL, and VGP pins.

The capacitive mode detection function is described further below. In the following descriptions, $Q_{(H)}$ represents the high-side power MOSFET, whereas $Q_{(L)}$ represents the low-side power MOSFET.

- **$Q_{(H)}$ Turn-on Period**

Figure 8-27 illustrates the RC pin waveform in the inductive area; Figure 8-28 illustrates the RC pin waveform in the capacitive area. In the inductance area, the RC pin voltage does not cross over $+V_{RC1}$ from high to low during the $Q_{(H)}$ turn-on period (see Figure 8-27).

Conversely, in the capacitive area, the RC pin voltage crosses over $+V_{RC1}$ from high to low. At this point, a capacitive mode operation is detected. Then, $Q_{(H)}$ is turned off, whereas $Q_{(L)}$ is turned on (see Figure 8-28).

- **$Q_{(L)}$ Turn-on Period**

Contrary to the $Q_{(H)}$ case, in the capacitive area, the RC pin voltage crosses over $-V_{RC1}$ from low to high during the $Q_{(L)}$ turn-on period. At this point, a capacitive mode operation is detected. Then, $Q_{(L)}$ is turned off, whereas $Q_{(H)}$ is turned on.

As explained above, the IC detects capacitive mode operations on a pulse-by-pulse basis, and prevents a capacitive mode operation.

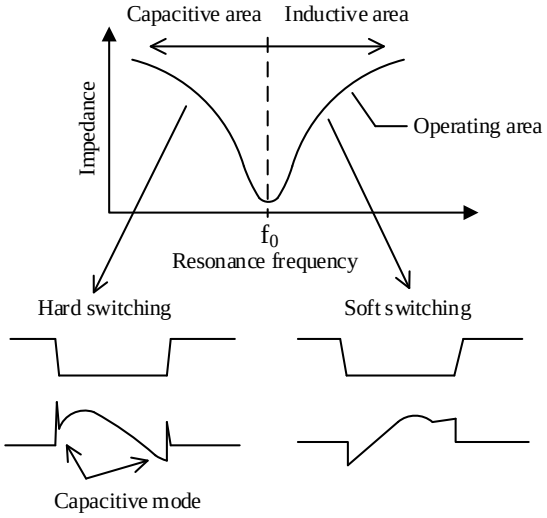


Figure 8-26. Operating Area of Resonant Power Supply

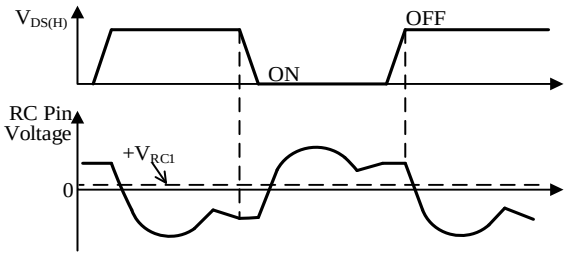


Figure 8-27. RC Pin Voltage Waveform in Inductive Area

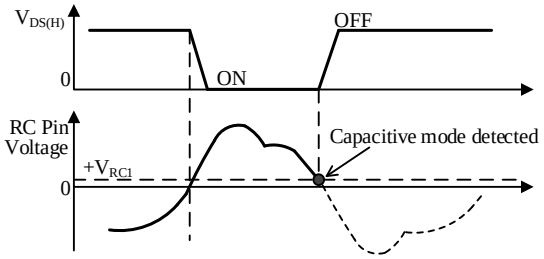


Figure 8-28. High-side Capacitive Mode Detection

There is no simplified method to obtain an accurate value of resonant current with parameters such as input and output conditions of the power supply. Therefore, C20 and R32 must be adjusted based on operation performance in an actual application. The peripheral constants of the RC pin are as follows:

- **C20, R32**

C20 should have a capacitance of 100 pF to 330 pF (about 1% of that of C22); R32 should have a resistance of about 100 Ω. R32 can be calculated with Equation (7). C20 and R32, which are used to detect the overcurrent and capacitive mode operations, must be set so that the absolute value of the RC pin voltage is higher than $|V_{RC1}| = 0.10$ V, and is within the absolute rating of ±6.0 V. The operation conditions prone to capacitive mode operation must also be taken into considerations in setting these components, including startup, supply input voltage turn-off, output shorted, and dynamic load effect on power system.

$$R32 \approx \frac{|V_{RC(S)}|}{I_{D(H)}} \times \left(\frac{C20 + C22}{C20}\right). \quad (7)$$

Where $V_{RC(S)}$ is the RC pin threshold voltage (fast; ±2.80 V), and $I_{D(H)}$ is the current at high-side power MOSFET turn-on.

- **C19, R31**

These are used for reducing high-frequency noise.

C19 should have a capacitance of 100 pF to 1000 pF; R31 should have a resistance of 100 Ω to 470 Ω.

8.16. LLC High-side Driver Undervoltage Lockout

The MD6751 incorporates the high-side driver undervoltage lockout (VB_UVLO) between the VB and VS pins.

When the voltage between the VB and VS pins (i.e., "VB–VS voltage") increases to $V_{BUV(ON)}$ = 6.8 V or more, the internal high-side driver starts operating. When the VB–VS voltage decreases to $V_{BUV(OFF)}$ = 6.4 V or less, the internal high-side driver stops operating. The VB_UVLO protects the IC in case both ends of the

capacitor C23 for bootstrap circuit and the protective diode D12 are shorted.

8.17. LLC Overcurrent Protection, LLC Overload Protection

The LLC overcurrent protection (LLC_OCP) detects a peak drain current of the power MOSFET on a pulse-by-pulse basis, and limits the output power. When the RC pin voltage reaches $V_{RC(L)}$ = ±1.75 V or more, the LCC_OCP is activated to increase oscillation frequency and thus limits the drain current. When the LCC_OCP condition persists for a period longer than a fixed OLP delay time, the LLC overload protection (LLC_OLP) is activated to stop the oscillation operations of the VGH, VGL, and VGP pins.

The RC pin voltage determines an appropriate OLP delay time: when $V_{RC} \geq V_{RC(L)}$, the delay time is set to $t_{RC(OLP)1}$ = 153.9 ms; when $V_{RC} \geq V_{RC(S)}$, the delay time is set to $t_{RC(OLP)2}$ = 1.99 ms.

During the LLC_OLP operation, the circuit current decreases to $I_{CC(P)}$ = 0.5 mA, and the bias assist function is disabled. When the VCC pin voltage decreases to $V_{CC(P.OFF)}$ = 8.3 V or less after the function disablement, the IC releases the LLC_OLP operation and restarts. In this way, the intermittent operation by the VCC_UVLO is repeated during the LLC_OLP operation. This intermittent operation reduces stresses on parts including power MOSFETs, secondary rectifier diodes, and so forth. In addition, the IC can reduce power consumption during this intermittent operation by employing a switching period shorter than a non-oscillating period.

When the causes of the overload condition are eliminated, the IC automatically returns to normal operation.

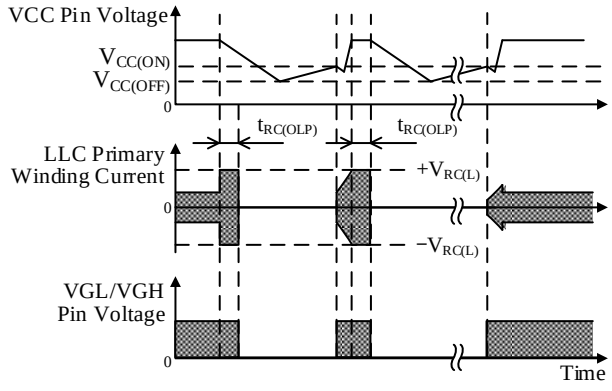


Figure 8-29. Operational Waveforms of LCC_OCP and LCC_OLP

8.18. Thermal Shutdown

When the control circuit temperature reaches $T_{J(TSD)}$ = 125 °C, the thermal shutdown (TSD) is activated. The IC then stops switching operation. In the condition where VCC ≤ $V_{CC(P.OFF)}$ of 8.3 V and the control circuit temperature falls below $T_{J(TSD)}$, the TSD circuit is activated again. During the TSD operation, the IC stops its operation. When the causes of the overheating condition are eliminated, the IC automatically returns to normal operation.

9. External Components

9.1. Resonant Transformer

The resonant power supply uses the leakage inductance of a transformer. Therefore, to reduce influences from eddy current and skin effect, use a bundle of fine litz wires as the wire of the transformer.

9.2. Inductor in PFC Stage

Apply proper design margin to temperature rise or magnetic saturation due to copper loss and iron loss.

9.3. Power MOSFET

Use a power MOSFET with a breakdown voltage, V_{DSS}, providing enough margin to the PFC output voltage, $V_{OUT(PFC)}$. Choose a proper size of heatsink which takes switching and on-resistance losses due to power MOSFETs into account.

9.4. PFC Boost Diode (D1, D2)

Choose a boost diode having a peak reverse voltage, V_{RSM}, which provides enough margin to the PFC output voltage, $V_{OUT(PFC)}$. A fast recovery diode with a short reverse recovery time, t_{rr}, is recommended to reduce noise and loss due to switching. Choose a proper size of heatsink which takes losses caused by forward voltage, V_F, and recovery current into considerations.

9.5. Output Capacitor (C3, C51)

Apply proper design margin to ripple current, ripple voltage, and temperature rise. A low-ESR capacitor is recommended to reduce ripple voltage, in terms of designing switch-mode power supplies.

9.6. Current-resonant Capacitor (C22)

Because large resonant current flows through C22, it should be a capacitor which supports high-current applications with small losses such as a polypropylene film capacitor. High-frequency current flows through C22; therefore, capacitor-specific frequency characteristics must also be taken into account.

10. PCB Pattern Layout

The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing. High-frequency and high-voltage current loops (see Figure 10-1) should be as small and wide as possible in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

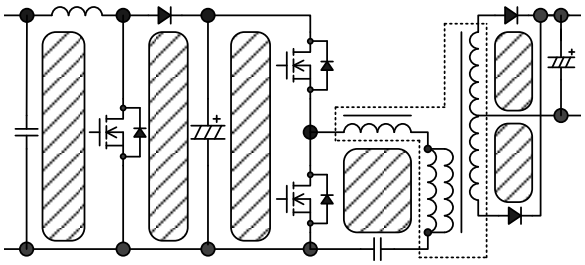


Figure 10-1. High-frequency Current Loop

Figure 10-2 is a peripheral circuit example of the IC.

The following considerations should be taken into account when designing pattern layouts for your application.

1) Main Circuit Trace Layout

Traces of the PFC and LLC circuits, where switching currents pass through, should be as wide and looped small as possible.

2) Logic Ground Trace Layout

If a large current flows through a logic ground, electric potential across the logic ground may vary and thus cause the IC to malfunction. Ground traces should be as wide and short as possible.

Logic ground traces should be designed as close as possible to the GND pin, at a single-point ground (or star ground) which is separated from the main circuit. Do not connect the PGND pin to these traces. Traces of the ground (i.e., the capacitors of the GND, PGND, and VCC pins) should be separately connected at a single-point ground whose connection is configured to the root of the output capacitor C3 in the PFC stage.

3) Peripheral Connections to VCC Pin

Traces connected to the VCC pin should be looped small as possible because the pin supplies power to the IC. If the IC and the electrolytic capacitor C13 are distant from each other, connect the film capacitor C11 (about 0.1 μF to 1.0 μF) between the VCC and GND pins with a minimal length of traces.

4) Peripheral Connections to VB Pin

The components of the bootstrap circuit connected between the VCC and VB pins (D13, R33) should be placed as close as possible to the IC. The capacitor C23 connected between the VB and VS pins should also be placed with a minimal length of traces.

5) Components for Logic Control System

These components should be placed close to the IC, and be connected to the corresponding pin of the IC with a minimal length of traces.

6) Secondary Rectifier Smoothing Circuit

This is the secondary main circuit in which switching current flows, should be wide and looped small as possible.

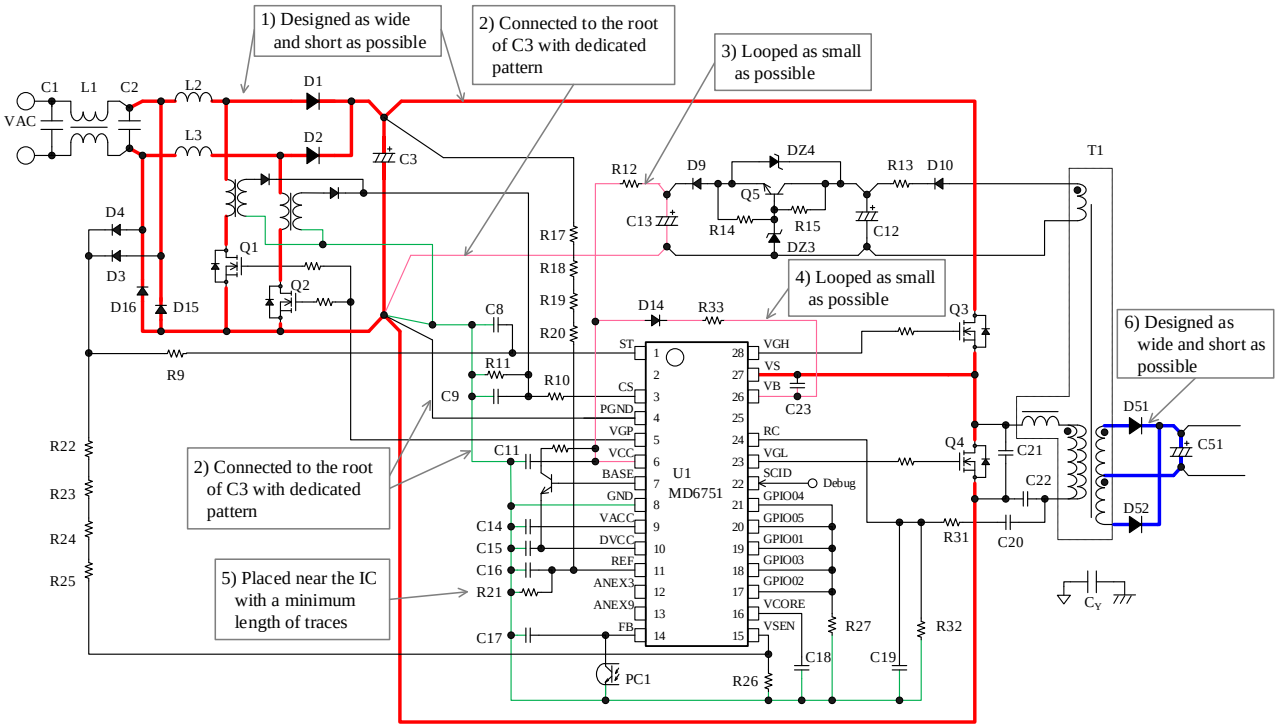


Figure 10-2. Example Connections to IC and Its Peripheral Circuits

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