100 V, 10 A, 50 mΩ
N-channel Power MOSFET Module

SHD4102

Data Sheet

Description

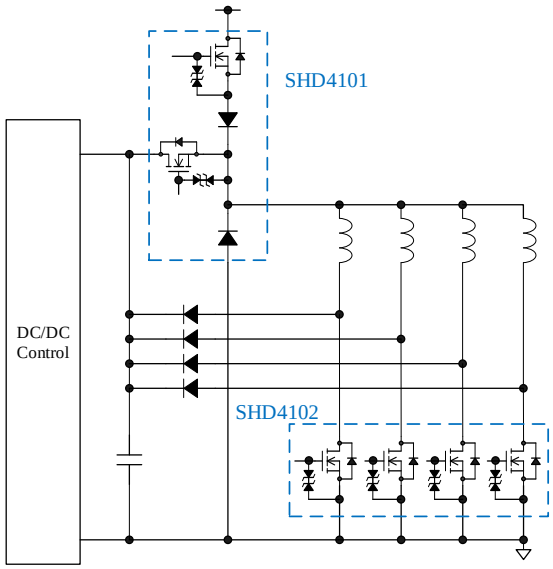
The SHD4102 includes four N-channel power MOSFETs in its small HSON package. The internal power MOSFETs have Zener diodes between gates and sources, thus requiring no externally clamped circuit for an injection coil drive circuit. Supplied in a low thermal resistance package, the product achieves high performance in heat dissipation.

Features

- Suitable for High Reliability Applications
- Complies with Automotive Quality Requirements
- AEC-Q101 Qualified
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Built-in Zener Diodes between Gates and Sources
- Low On-resistance
- Specifications (Q1 to Q4)
  $V_{(BR)DSS}$ ---------- 100 V (I_D = 100 μA)
  I_D ---------- 10 A
  $R_{DS(ON)}$ ---------- 50 mΩ max. (I_D = 5 A, V_{GS} = 10 V)

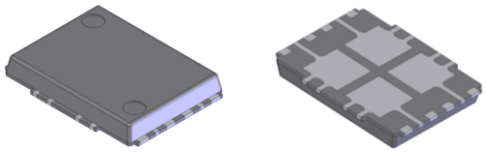
Typical Application

- **Solenoid Injection System**



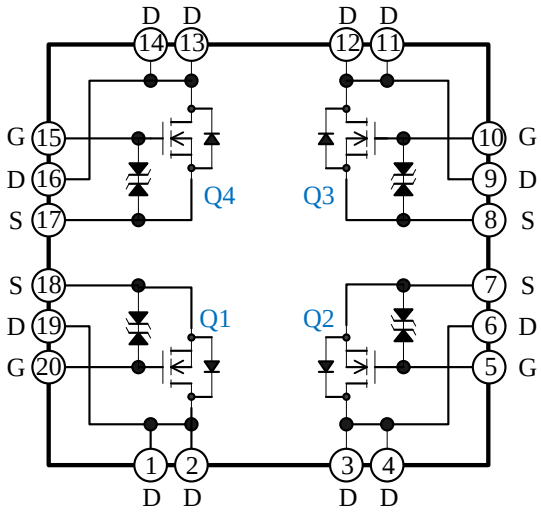
Package

- HSON-20



Not to scale

Internal Schematic Diagram



D: Drain
S: Source
G: Gate

Applications

- Injection Coil Driver Circuits

Absolute Maximum Ratings

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit
Drain-to-Source Voltage	V_{DS}		100	V
Gate-to-Source Voltage	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C = 25 °C	10	A
Pulsed Drain Current	I_{DM}	t ≤ 30 µs, duty cycle ≤ 1 %	30	A
Single Pulse Avalanche Energy	E_{AS}	V_{DD} = 14 V, L = 1.08 mH, I_D = 10 A, unclamped, R_G = 50 Ω; see Figure 16	62.5	mJ
Avalanche Current	I_{AS}		10	A
Drain-to-Source dv/dt 1	dv/dt 1	See Figure 16	0.6	V/ns
Peak Diode Recovery dv/dt 2	dv/dt 2	See Figure 17	5	V/ns
Peak Diode Recovery di/dt	di/dt	See Figure 17	100	A/µs
Power Dissipation	P_D	T_C = 25 °C, all elements operating; mounted on an FR4 board (26 mm × 36 mm × 1.66 mm)	1.7	W
		T_C = 25 °C, all elements operating; with an infinite heatsink	80	W
Junction Temperature	T_J		150	°C
Storage Temperature	T_{STG}		−55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	T_C = 25 °C, all elements operating; with an infinite heatsink	—	—	6.25	°C/W

Electrical Characteristics

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	100	—	—	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	µA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = ± 15 V	—	—	± 10	µA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 5 A	9	—	—	S
Static Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 5 A, V_{GS} = 10 V	—	38	50	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	2200	—	pF
Output Capacitance	C_{oss}		—	210	—	
Reverse Transfer Capacitance	C_{rss}		—	110	—	
Total Gate Charge	Q_g	V_{DD} = 50 V, I_D = 5 A, V_{GS} = 10 V, R_L = 10 Ω	—	45	—	nC
Gate-to-Source Charge	Q_{gs}		—	6	—	
Gate-to-Drain Charge	Q_{gd}		—	10	—	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 5 A, V_{GS} = 10 V, R_G = 20 Ω, R_L = 10 Ω; see Figure 18	—	30	—	ns
Rise Time	t_r		—	40	—	
Turn-off Delay Time	$t_{d(off)}$		—	160	—	
Fall Time	t_f		—	80	—	
Source-to-Drain Diode Forward Voltage	V_{SD}	I_S = 10 A, V_{GS} = 0 V	—	—	1.2	V
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	I_F = 10 A, di/dt = 100 A/µs; see Figure 17	—	50	—	ns

Rating and Characteristic Curves

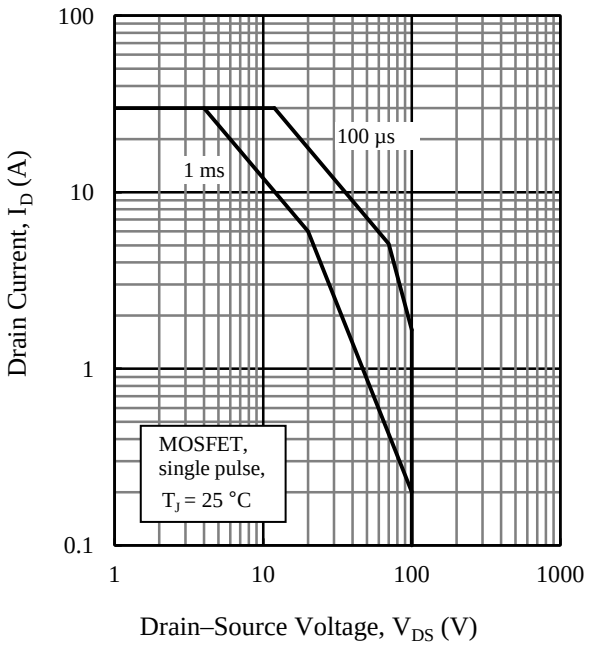


Figure 1. Q3: Safe Operating Area

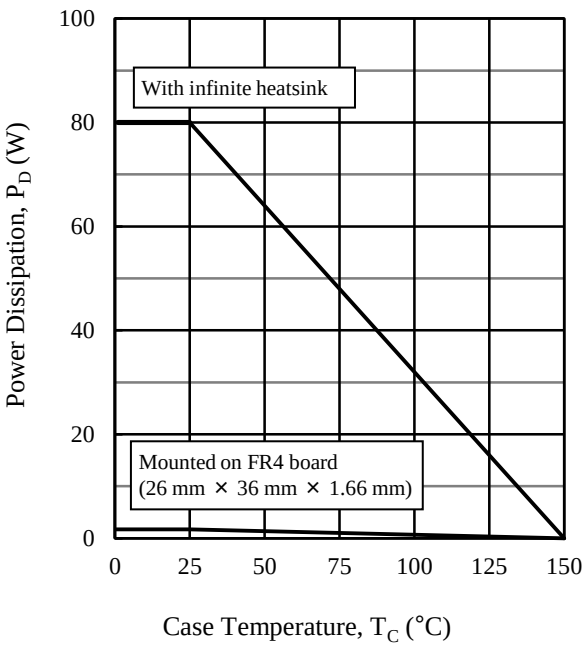


Figure 2. Q3: Power Dissipation vs. Case Temperature

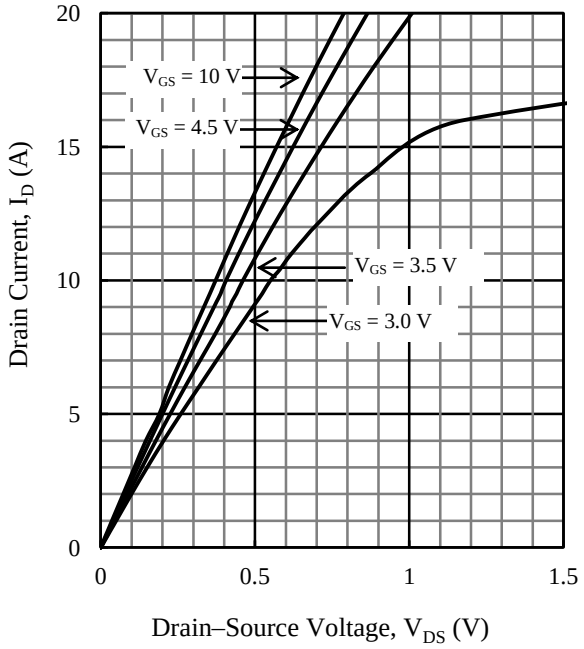


Figure 3. Q3: Output Characteristics (T_J = 25 °C)

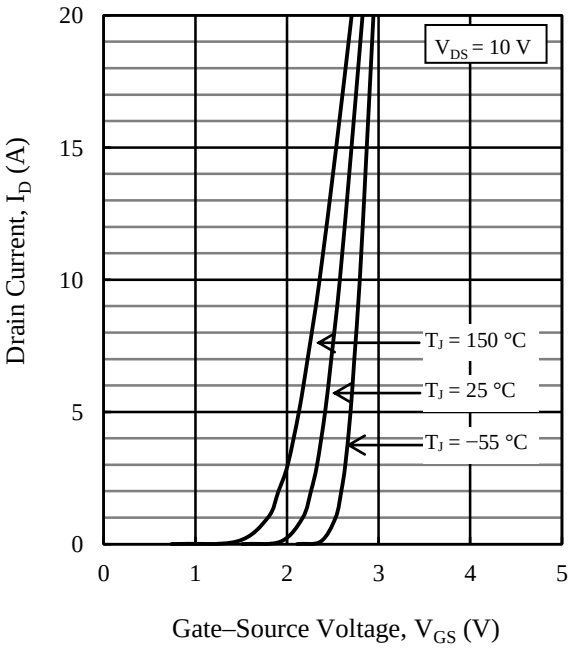


Figure 4. Q3: Transfer Characteristics

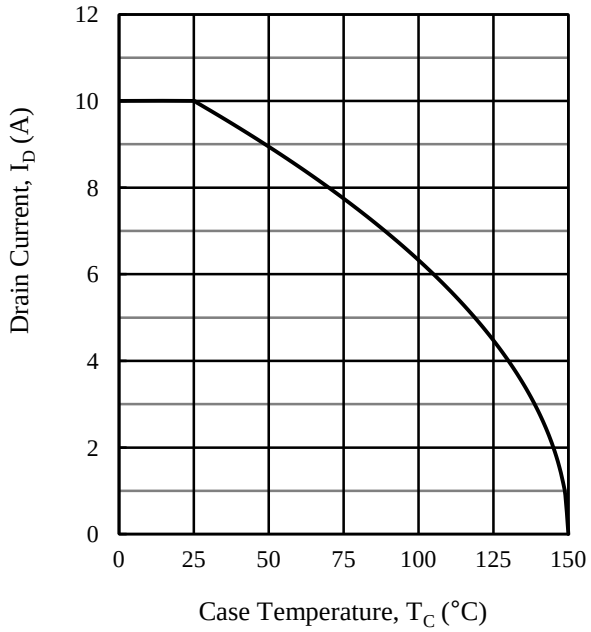


Figure 5. Q3: Drain Current vs. Case Temperature

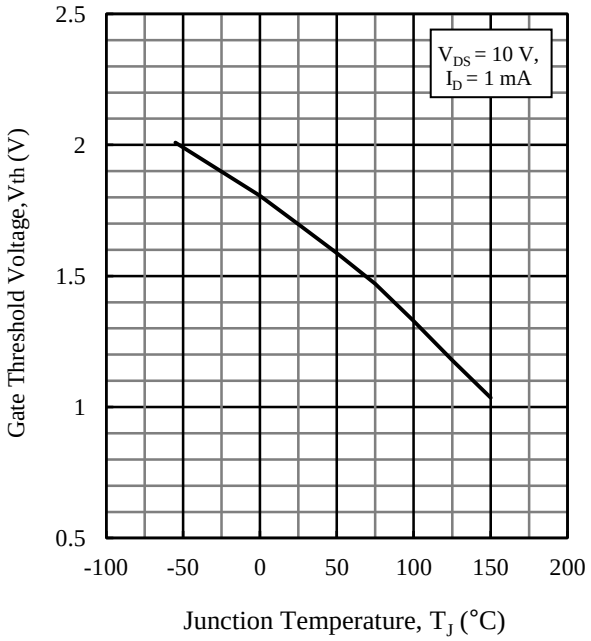


Figure 6. Q3: Gate Threshold Voltage vs. Junction Temperature

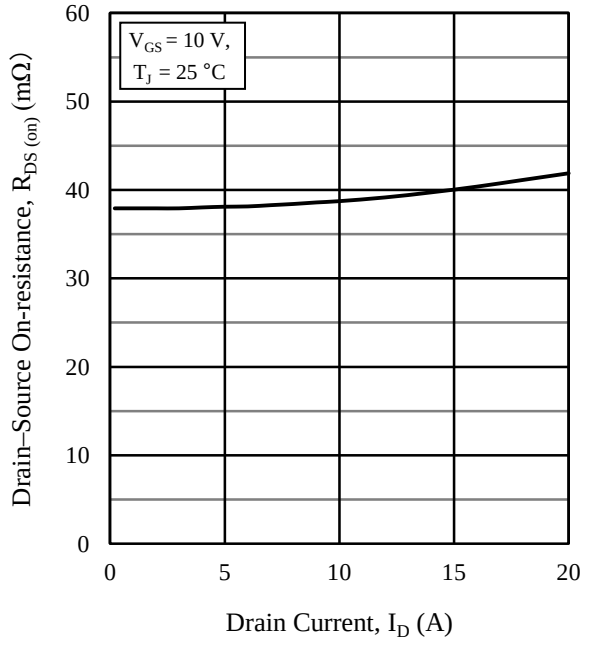


Figure 7. Q3: Drain–Source On-resistance vs. Drain Current

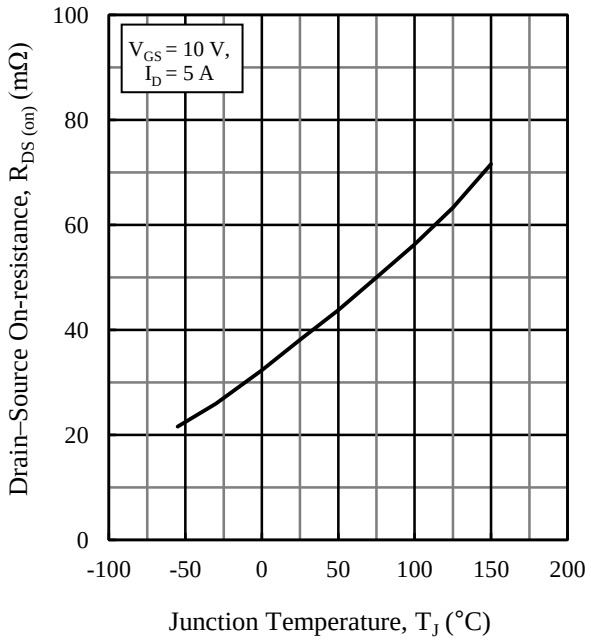


Figure 8. Q3: Drain–Source On-resistance vs. Junction Temperature

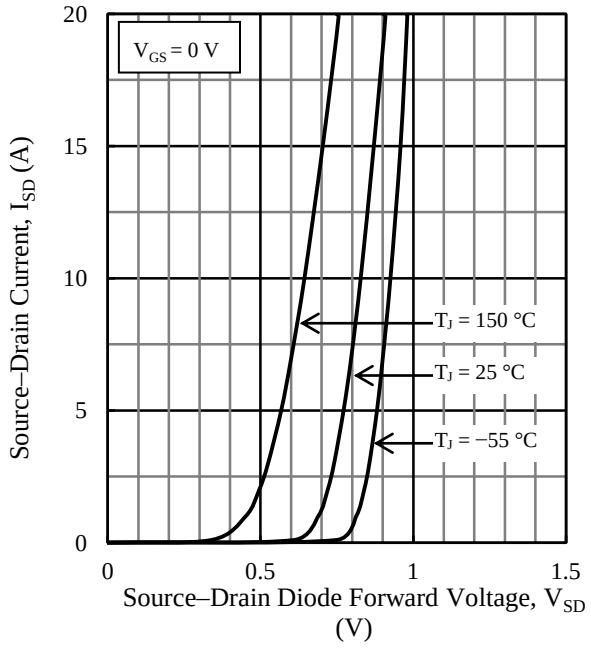


Figure 9. Q3: Forward Diode Characteristics

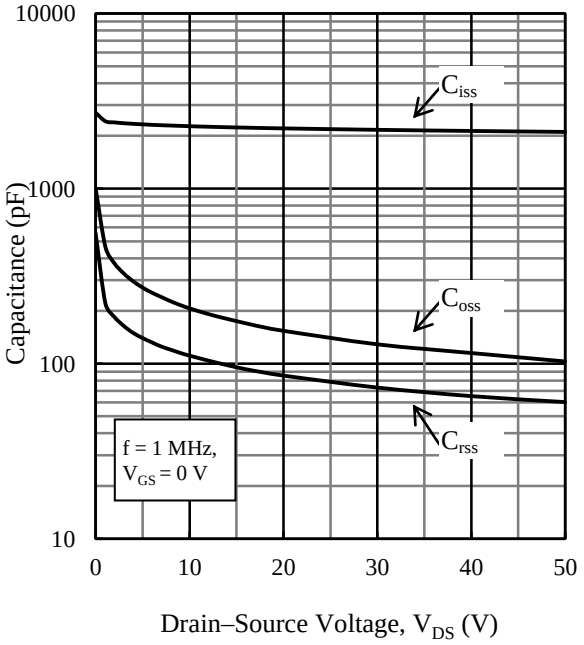


Figure 10. Q3: Capacitance Characteristics

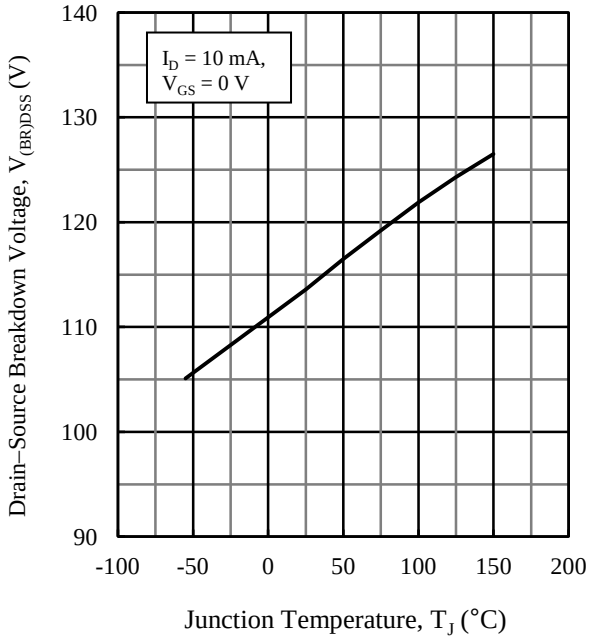


Figure 11. Q3: Drain-Source Breakdown Voltage vs. Junction Temperature

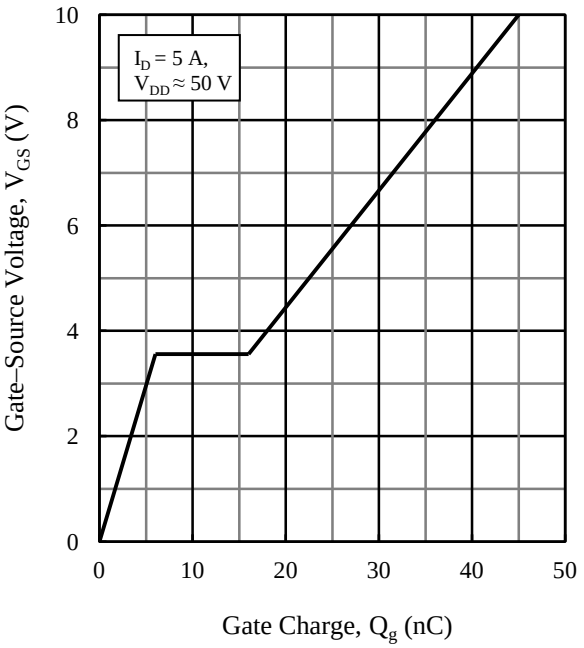


Figure 12. Q3: Typical Gate Charge

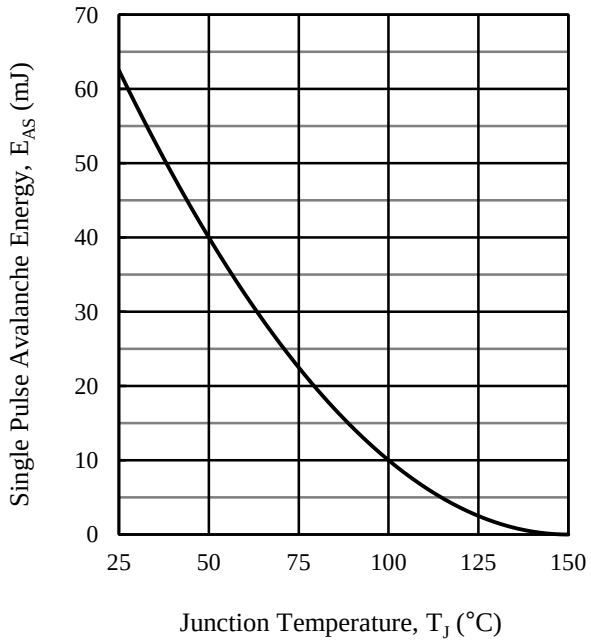


Figure 13. Q3: Typical Avalanche Energy

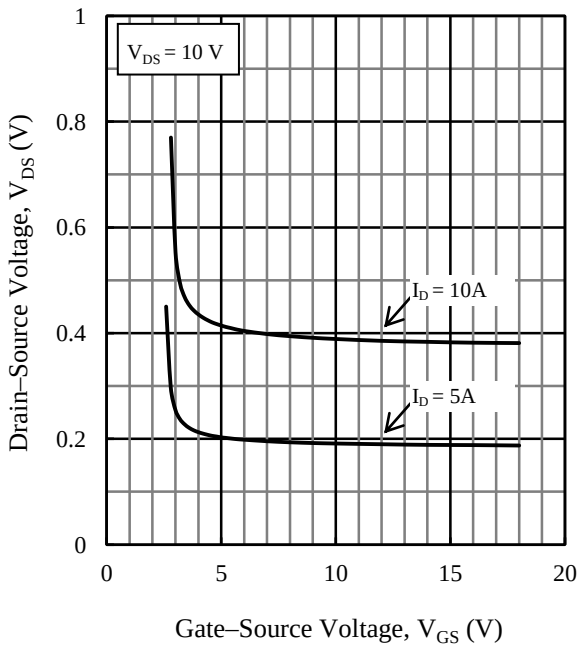


Figure 14. Q3: Transfer Characteristics

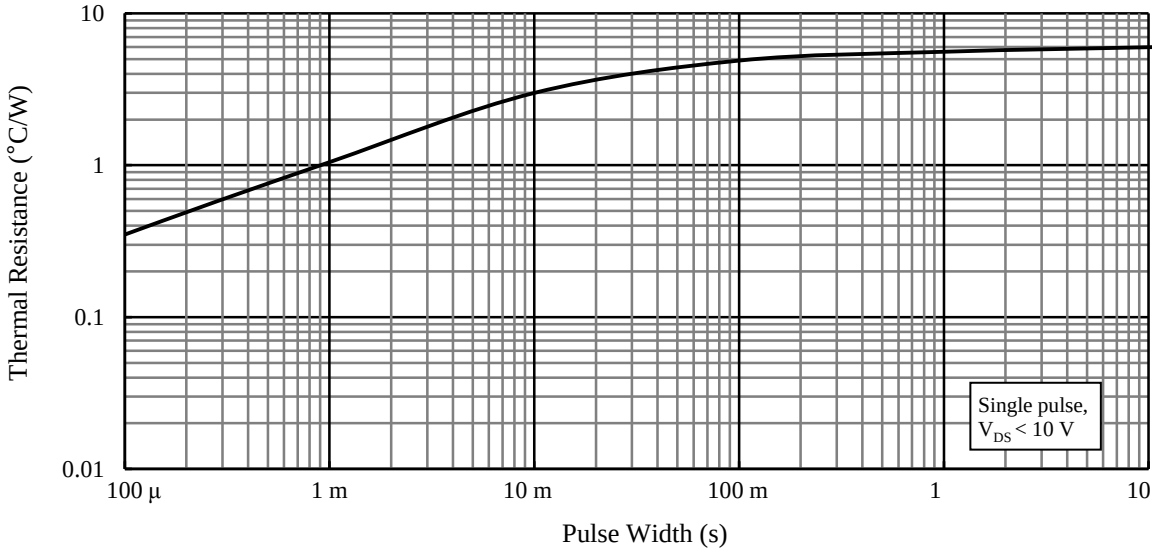
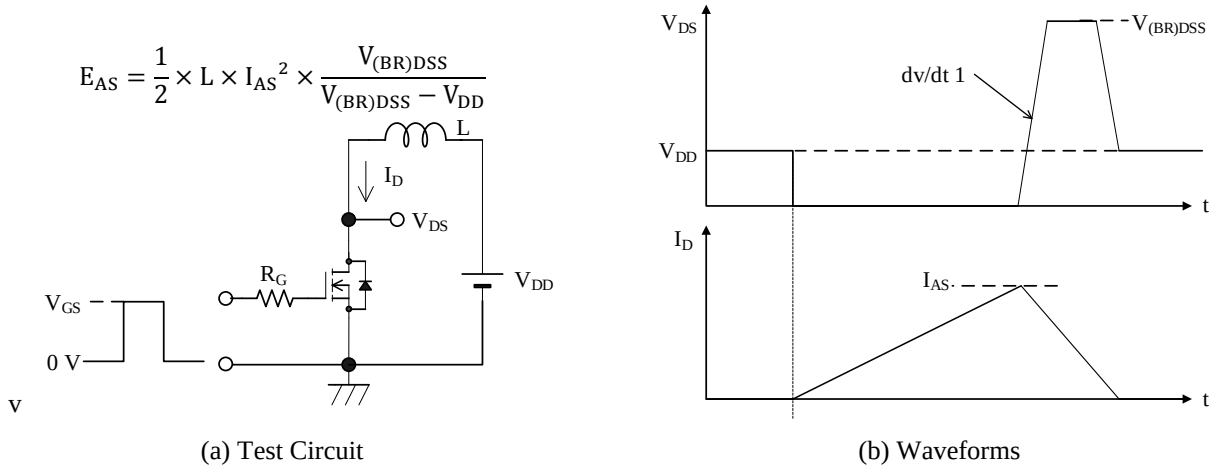


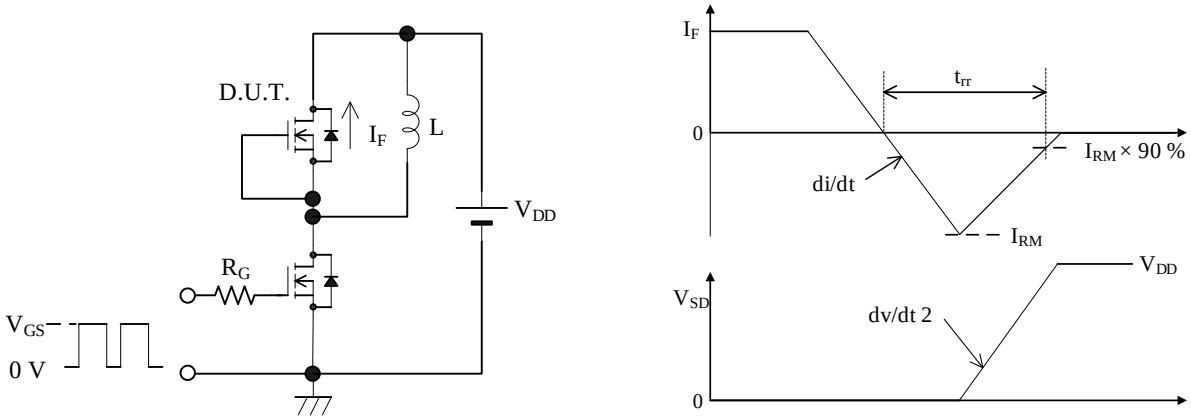
Figure 15. Q3: Transient Thermal Resistance

Test Circuits and Waveforms



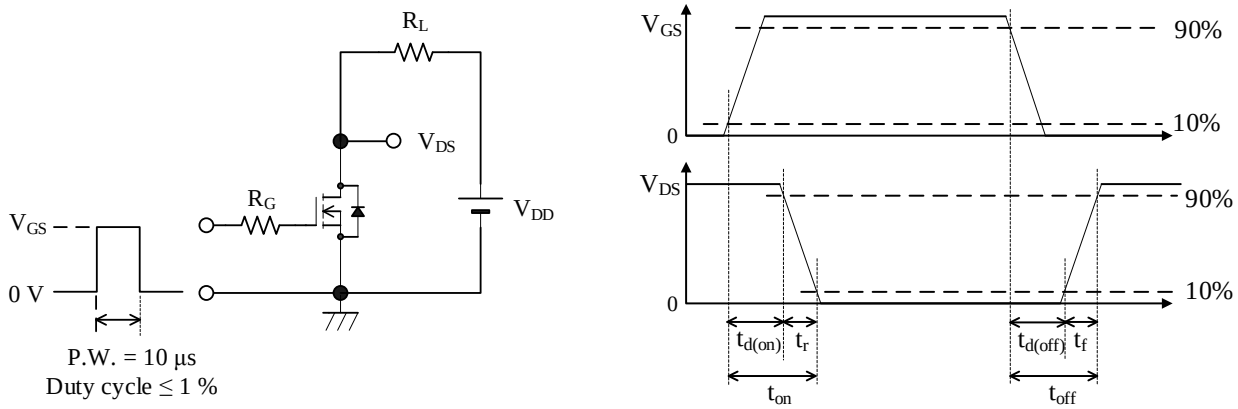
(a) Test Circuit (b) Waveforms

Figure 16. Unclamped Inductive Test Circuit and Switching Time Waveforms



(a) Test Circuit (b) Waveforms

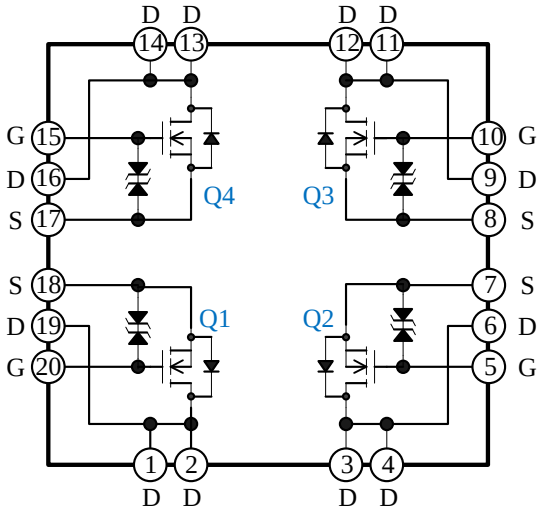
Figure 17. Diode Reverse Recovery Time



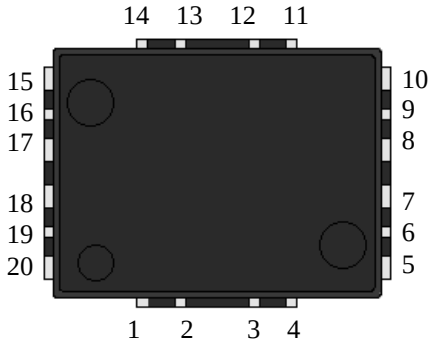
(a) Test Circuit (b) Waveforms

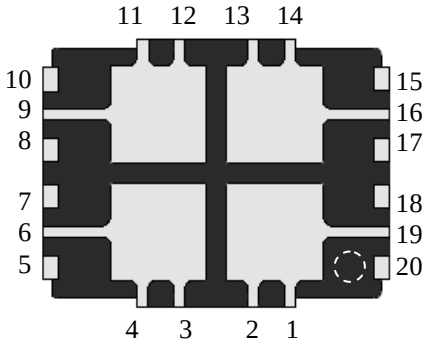
Figure 18. Resistive Load Test Circuit and Switching Time Waveforms

Internal Schematic Diagram



Pin Configuration Definitions

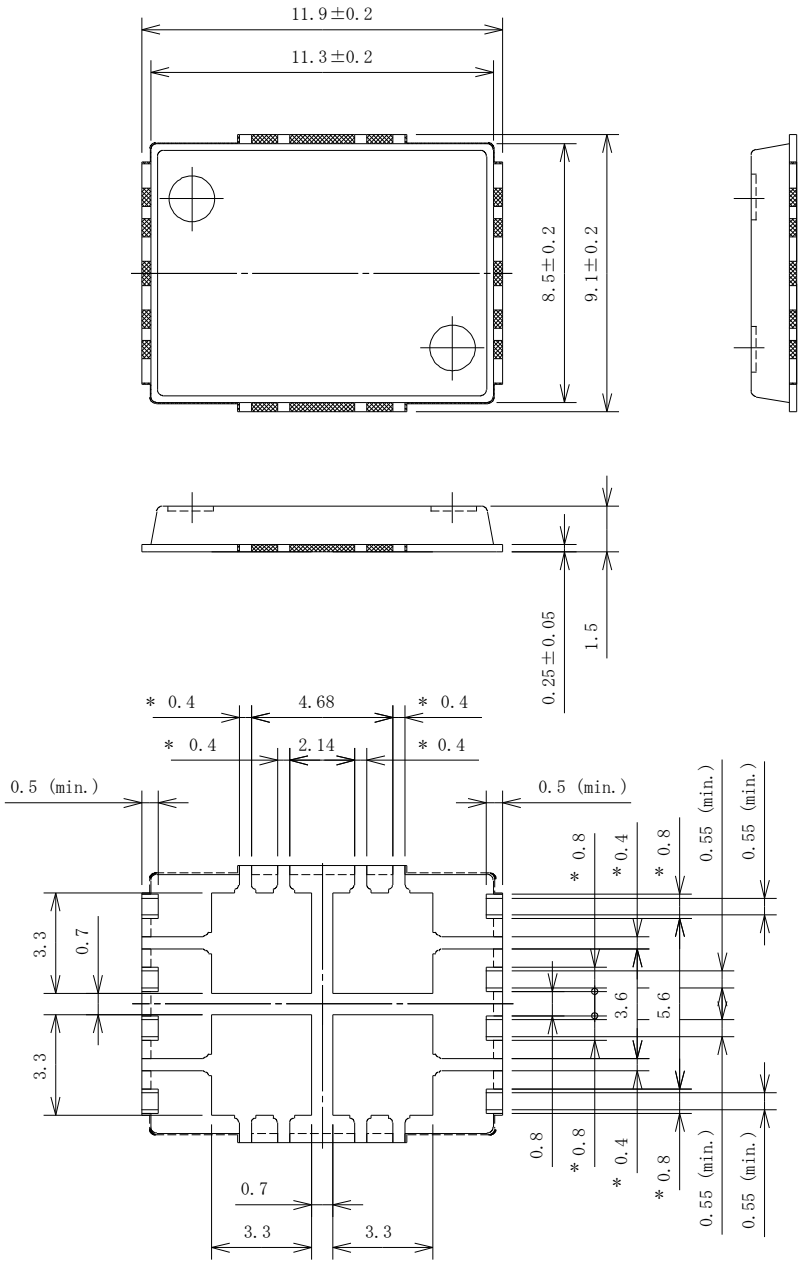




Pin Number	Description	Pin Number	Description
1	Q1 drain	11	Q3 drain
2	Q1 drain	12	Q3 drain
3	Q2 drain	13	Q4 drain
4	Q2 drain	14	Q4 drain
5	Q2 gate	15	Q4 gate
6	Q2 drain	16	Q4 drain
7	Q2 source	17	Q4 source
8	Q3 source	18	Q1 source
9	Q3 drain	19	Q1 drain
10	Q3 gate	20	Q1 gate

Physical Dimensions

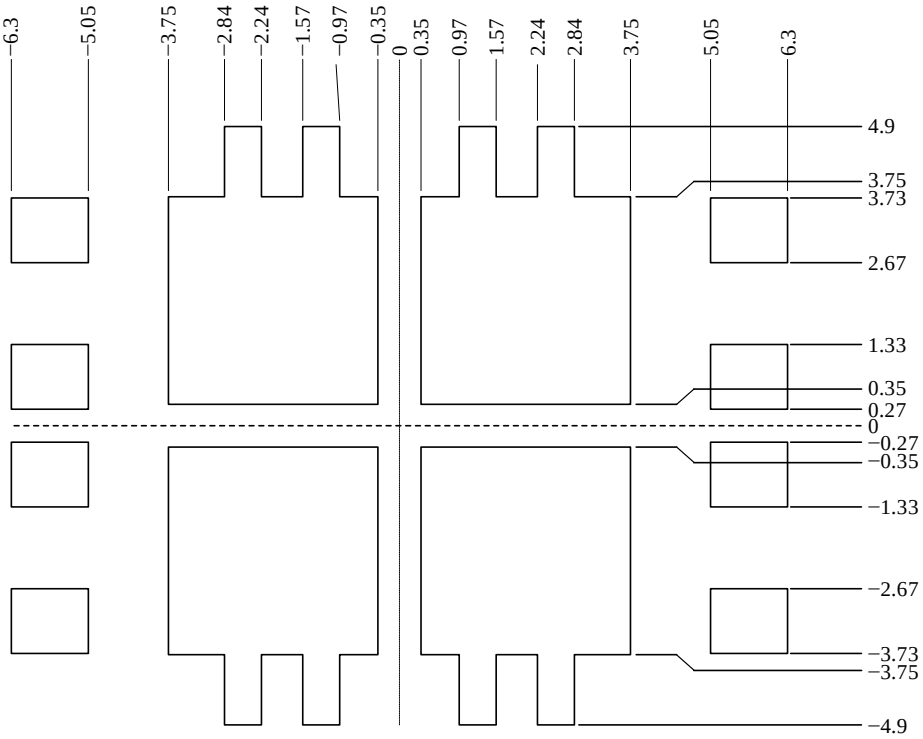
● **HSON-20 Package**



NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Dimensions with the asterisks do not include any mold flash.
- ▨ depicts the area where one or more mold flashes similar in thickness to that of the frame may exist.
- Dimensions without tolerances have a tolerance of ±0.1.
- When soldering the products, it is required to minimize the working time within the following limits:
  Reflow
  Preheat: 180 °C / 90 ± 30 s
  Solder heating: 250 °C / 10 ± 1s, 2 times (260 °C peak)
  Soldering iron: 380 ± 10 °C / 3.5 ± 0.5 s, 1 time
- The following pins are not guaranteed to be connected by soldering: 6, 9, 16, and 19.

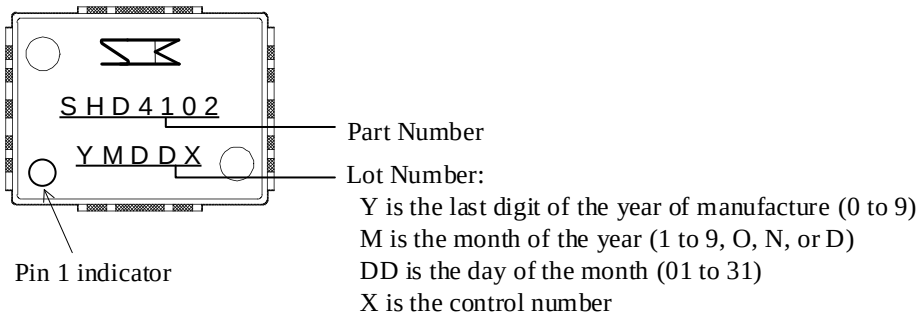
● **HSON-20 Land Pattern Example**



NOTE:

- Dimensions in millimeters

Marking Diagram



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DSGN-AEZ-16003