100 V, 10 A, 50 mΩ
Power MOSFET Module

SHD4115

Data Sheet

Description

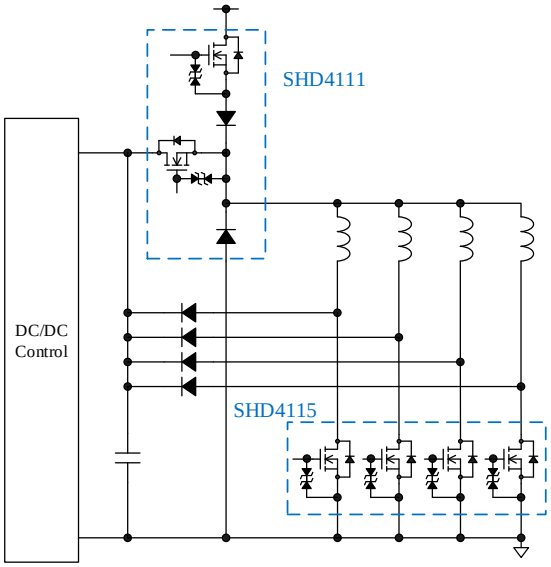
The SHD4115 includes four N-channel power MOSFETs in its small HSON package. The internal power MOSFETs have Zener diodes between gates and sources, thus requiring no externally clamped circuit for an injection coil drive circuit. Supplied in a low thermal resistance package, the product achieves high performance in heat dissipation. In addition, its HSON package employs a wettable flank structure, with the pin tips plated and the case resin around the pins grooved. This achieves higher reliability in mounting.

Features

- High Reliability Achieved
- Automotive Requirements Satisfied
- AEC-Q101 Qualified
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Wettable Flank HSON Package
- Case Resin around the Pins Grooved
- Built-in Zener Diodes between Gates and Sources
- Specifications (Q1 to Q4)
  $V_{(BR)DSS}$ ---------- 100 V (I_D = 100 μA)
  I_D ---------- 10 A
  $R_{DS(ON)}$ ---------- 50 mΩ max. (I_D = 5 A, V_{GS} = 10 V)

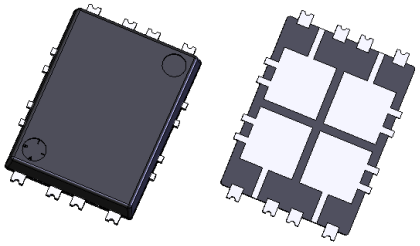
Typical Application

- **Solenoid Injection System**



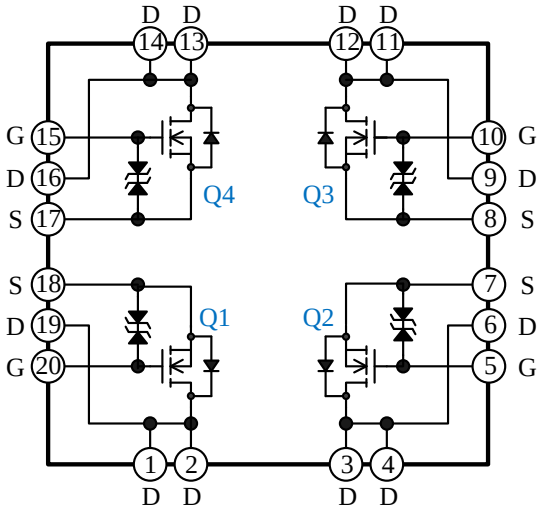
Package

- HSON-20



Not to scale

Internal Schematic Diagram



D: Drain
S: Source
G: Gate

Application

- Injection Coil Driver Circuits

Absolute Maximum Ratings

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit
Drain-to-Source Voltage	V_{DS}		100	V
Gate-to-Source Voltage	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C = 25 °C	10	A
Pulsed Drain Current	I_{DM}	t ≤ 30 µs, duty cycle ≤ 1 %	30	A
Power Dissipation	P_D	T_C = 25 °C, all power MSOFETs operating; mounted on an FR4 board (26 mm × 36 mm × 1.66 mm)	1.7	W
		T_C = 25 °C, all power MSOFETs; with an infinite heatsink	80	W
Avalanche Energy	E_{AS}	Single pulse, V_{DD} = 14 V, L = 1.0 mH, I_D = 10 A, unclamped, R_G = 50 Ω; see Figure 16	62.5	mJ
Avalanche Current	I_{AS}		10	A
Maximum Drain-to-Source dv/dt	dv/dt1	V_{DD} = 14 V, L = 1.08 mH, I_D = 10 A, unclamped, R_G = 50 Ω; see Figure 16	0.6	V/ns
Maximum Diode Recovery dv/dt	dv/dt2	See Figure 17	5	V/ns
Maximum Diode Recovery di/dt	di/dt	See Figure 17	100	A/µs
Junction Temperature	T_J		150	°C
Storage Temperature	T_{STG}		−55 to 150	°C

Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	T_C = 25 °C; with an infinite heatsink	—	—	6.25	°C/W

Electrical Characteristics

Unless otherwise specified, T_A = 25 °C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 100 µA, V_{GS} = 0 V	100	—	—	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	µA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = ±15 V	—	—	± 10	µA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 5 A	9	—	—	S
Static Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 5 A, V_{GS} = 10 V	—	38	50	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	2200	—	pF
Output Capacitance	C_{oss}		—	210	—	
Reverse Transfer Capacitance	C_{rss}		—	110	—	
Total Gate Charge	Q_G	V_{DD} = 50 V, I_D = 5 A, V_{GS} = 10 V, R_L = 10 Ω	—	45	—	nC
Gate-to-Source Charge	Q_{GS}		—	6	—	
Gate-to-Drain Charge	Q_{GD}		—	10	—	
Turn-on Delay Time	$t_{d(ON)}$	V_{DD} = 50 V, I_D = 5 A, V_{GS} = 10 V, R_G = 20 Ω, R_L = 10 Ω; see Figure 18	—	30	—	ns
Turn-on Rise Time	t_r		—	40	—	
Turn-off Delay Time	$t_{d(OFF)}$		—	160	—	
Turn-off Fall Time	t_f		—	80	—	
Source-to-Drain Diode Forward Voltage Drop	V_{SD}	I_S = 10 A, V_{GS} = 0 V	—	—	1.2	V
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	I_S = 10 A, di/dt = 100 A/µs; see Figure 17	—	50	—	ns

Derating Curves

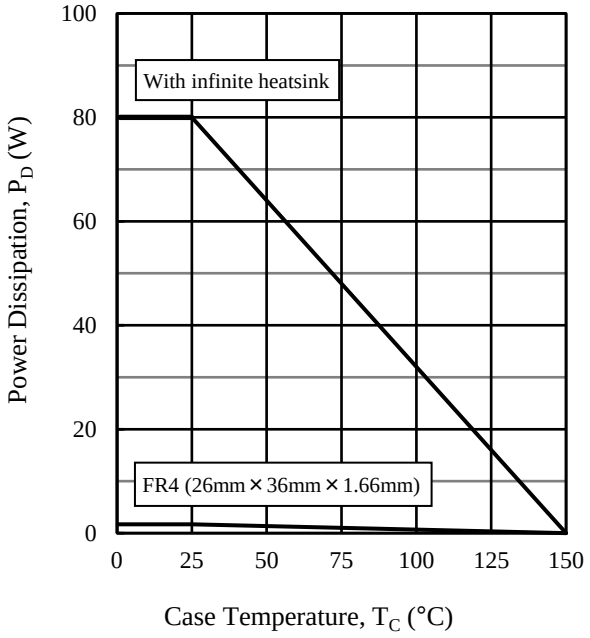


Figure 1. P_D vs. T_C
(All Power MOSFETs Operating)

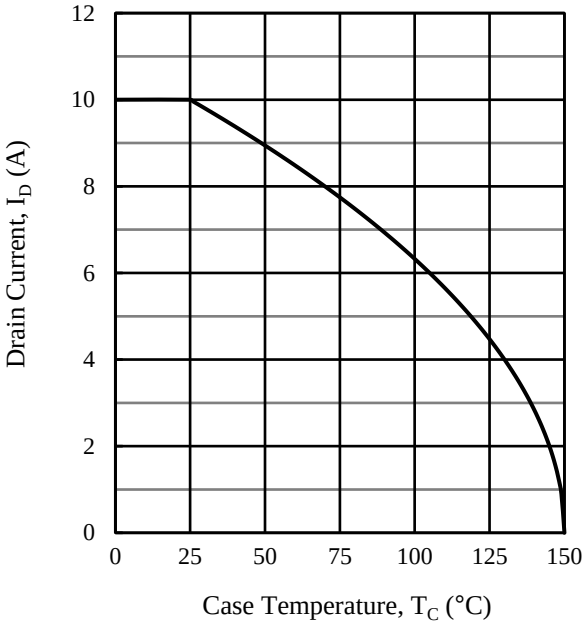


Figure 2. I_D vs. T_C

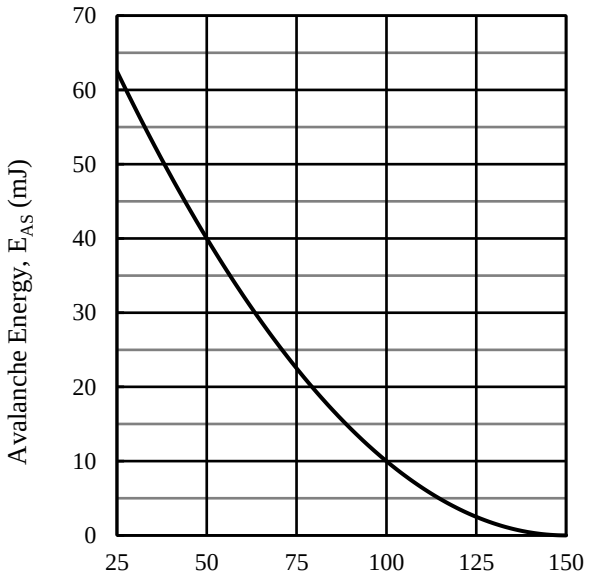


Figure 3. E_{AS} vs. T_J (Single Pulse)

Characteristic Curves

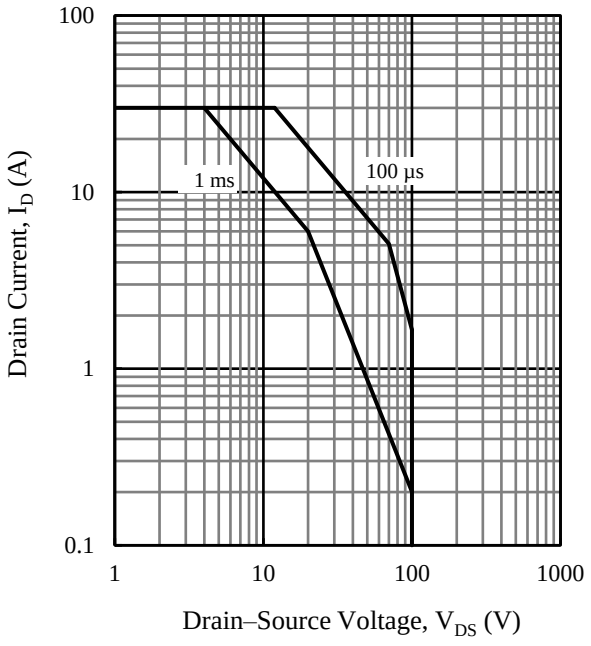


Figure 4. Typical Characteristics: Safe Operating Area (Single Pulse, T_J = 25 °C)

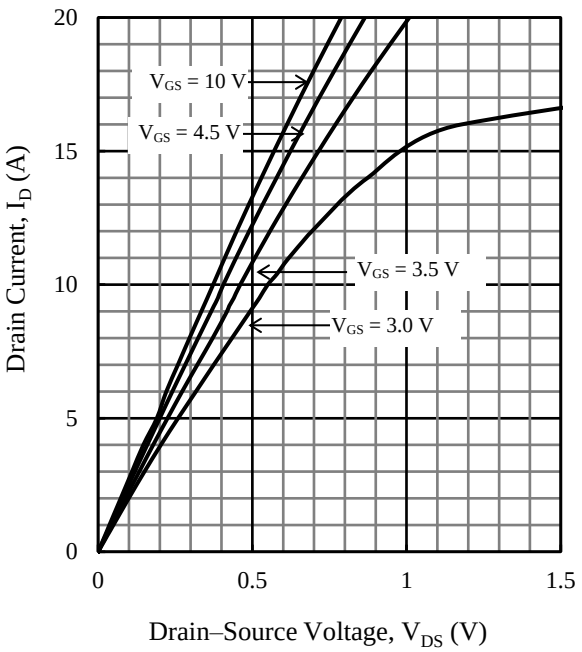


Figure 5. Typical Characteristics: I_D vs. V_{DS} (T_J = 25 °C)

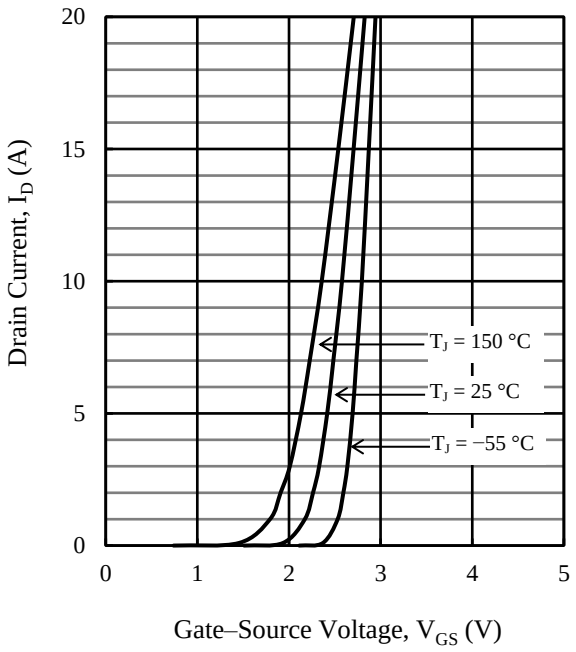


Figure 6. Typical Characteristics: I_D vs. V_{GS} (V_{DS} = 10 V)

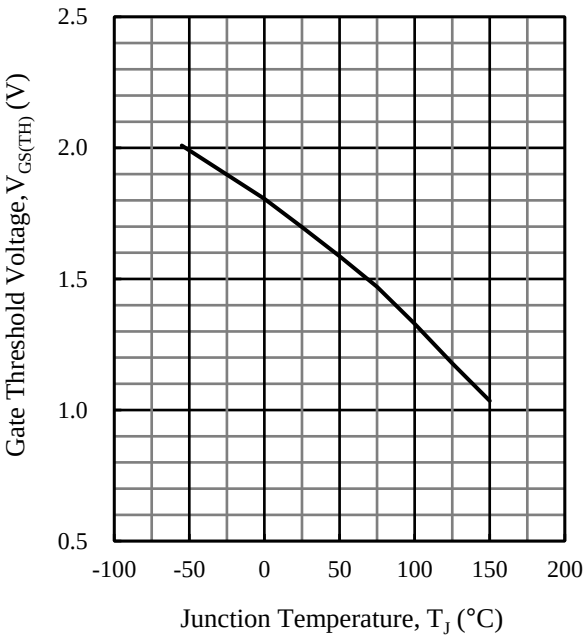


Figure 7. Typical Characteristic: $V_{GS(TH)}$ vs. T_J (V_{DS} = 10 V, I_D = 1 mA)

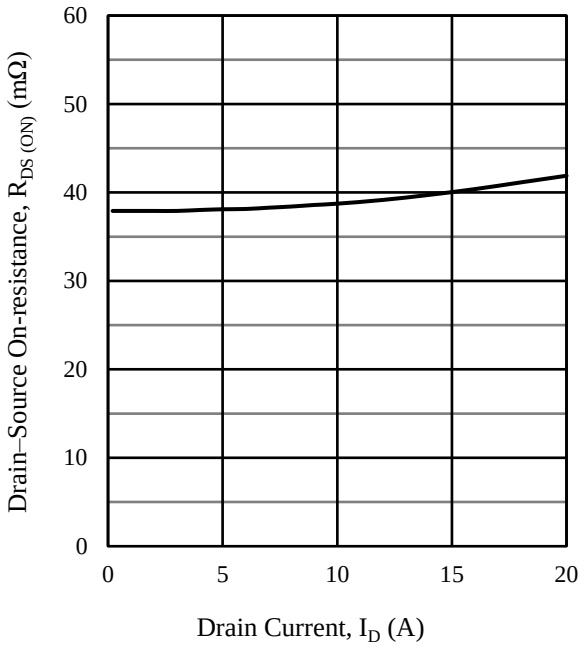


Figure 8. Typical Characteristic:
$R_{DS(ON)}$ vs. I_D (V_{GS} = 10 V, T_J = 25 °C)

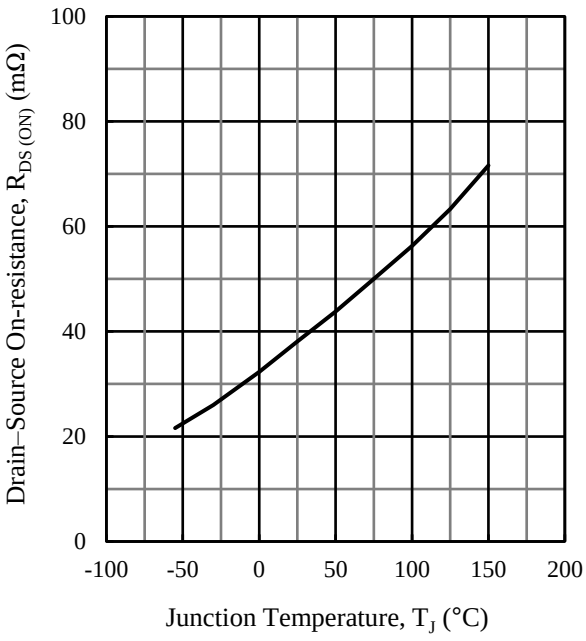


Figure 9. Typical Characteristic:
$R_{DS(ON)}$ vs. T_J (V_{GS} = 10 V, I_D = 5 A)

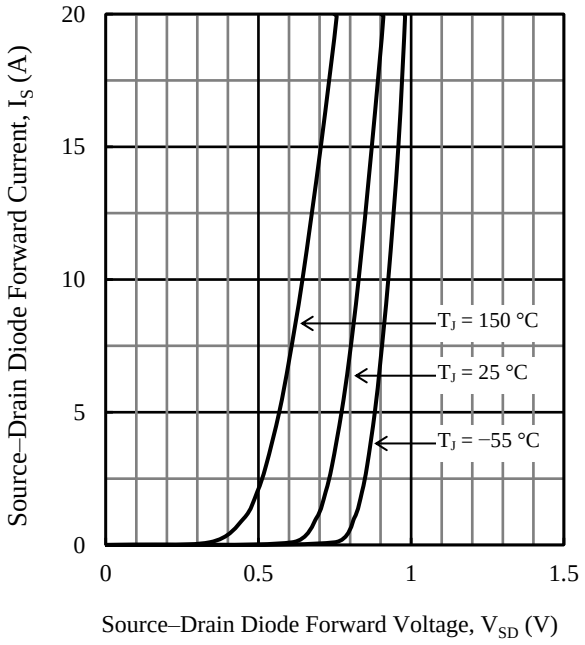


Figure 10. Typical Characteristics:
I_S vs. V_{SD} (V_{GS} = 0 V)

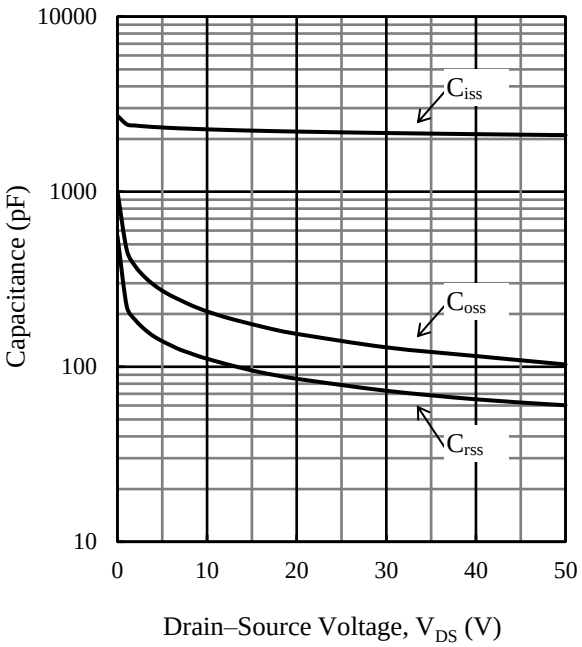


Figure 11. Typical Characteristics:
Capacitance vs. V_{DS} (f = 1 MHz, V_{GS} = 0 V)

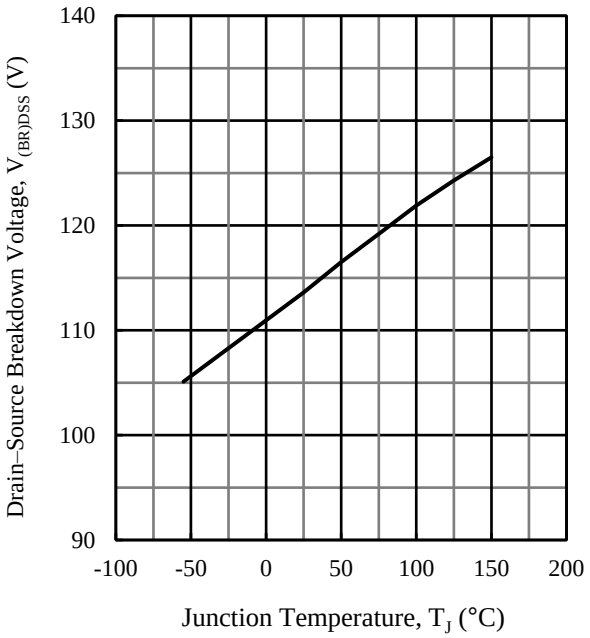


Figure 12. Typical Characteristic:
$V_{(BR)DSS}$ vs. T_J (I_D = 10 mA, V_{GS} = 0 V)

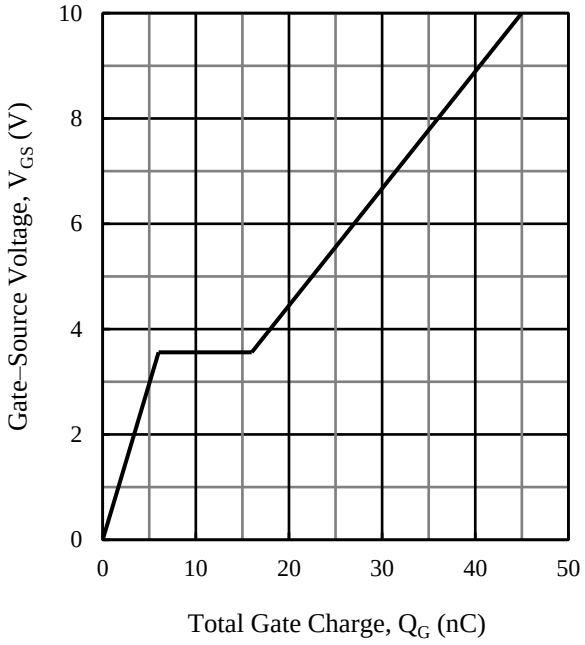


Figure 13. Typical Characteristic:
V_{GS} vs. Q_G (I_D = 5 A, V_{DD} ≈ 50 V)

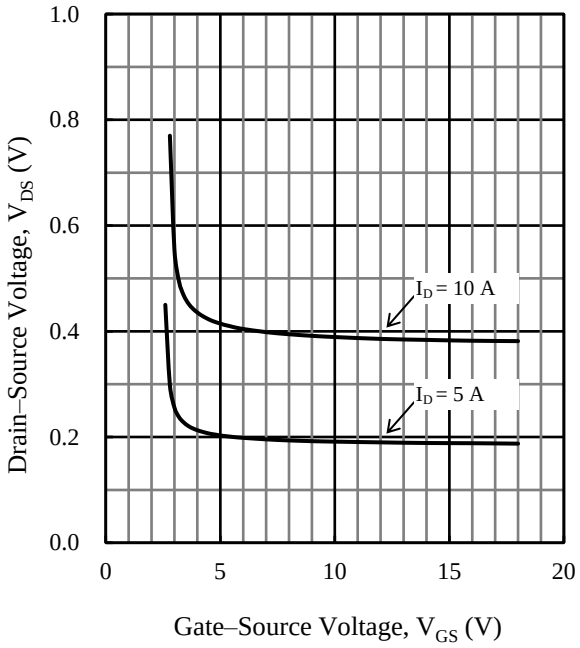


Figure 14. Typical Characteristics:
V_{DS} vs. V_{GS} (V_{DS} = 10 V)

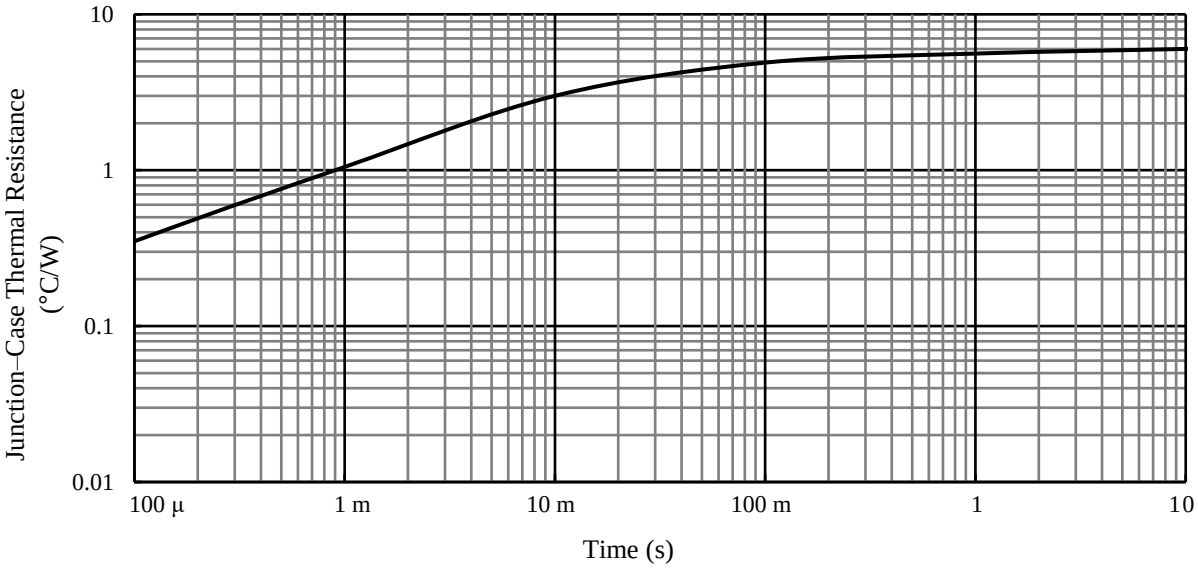
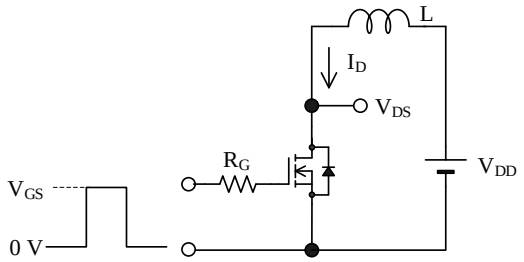
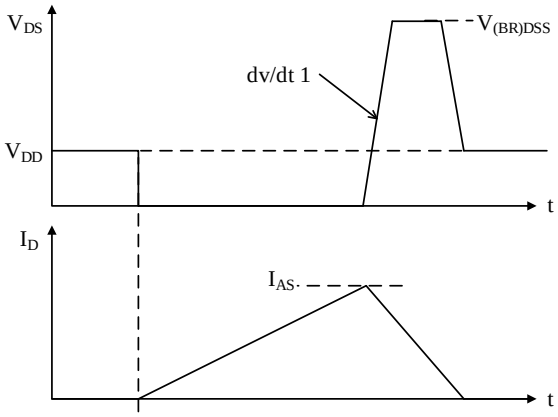


Figure 15. Transient Thermal Resistance Characteristic (Single Pulse, T_C = 25 °C, V_{DS} < 10 V)

$$E_{AS} = \frac{1}{2} \times L \times {I_{AS}}^2 \times \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

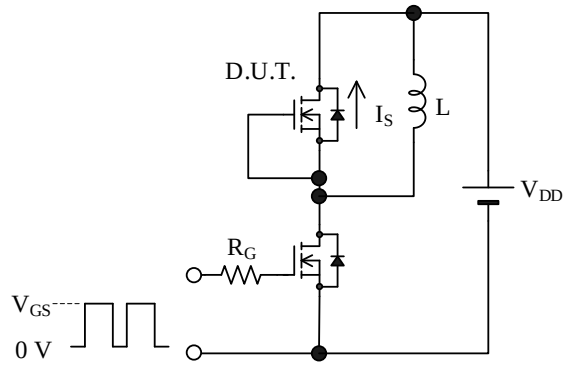


(a) Test Circuit

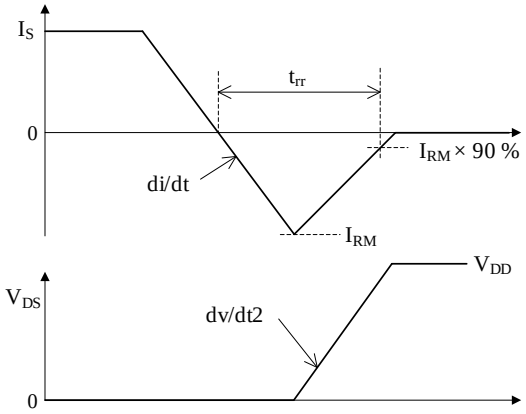


(b) Waveforms

Figure 16. Avalanche Energy and dv/dt1 Test

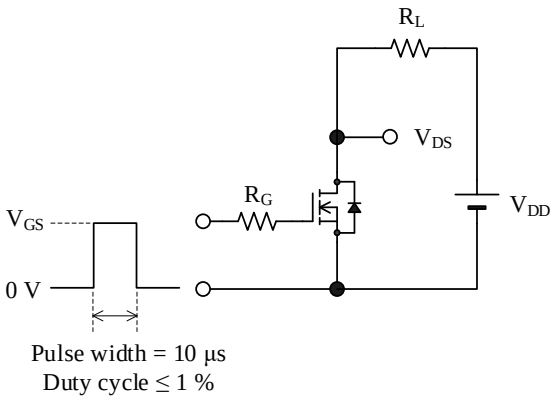


(a) Test Circuit

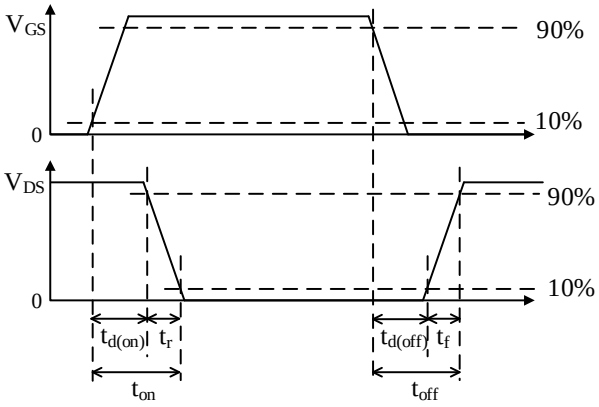


(b) Waveforms

Figure 17. Diode Reverse Recovery Time Test



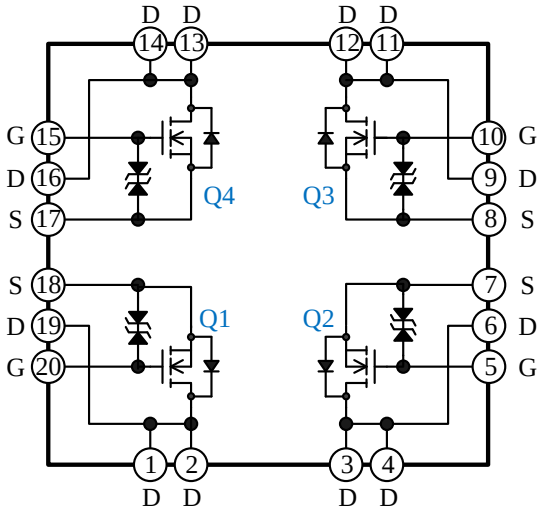
(a) Test Circuit



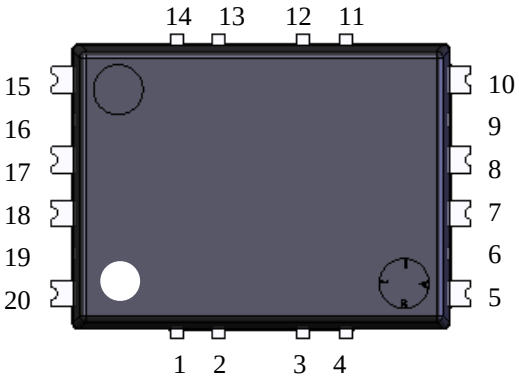
(b) Waveforms

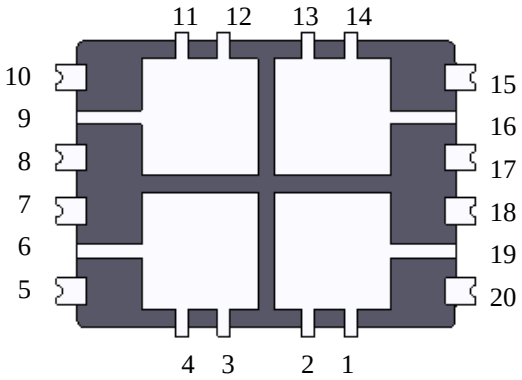
Figure 18. Resistive Load Switching Time Test

Internal Schematic Diagram



Pin Configuration Definitions

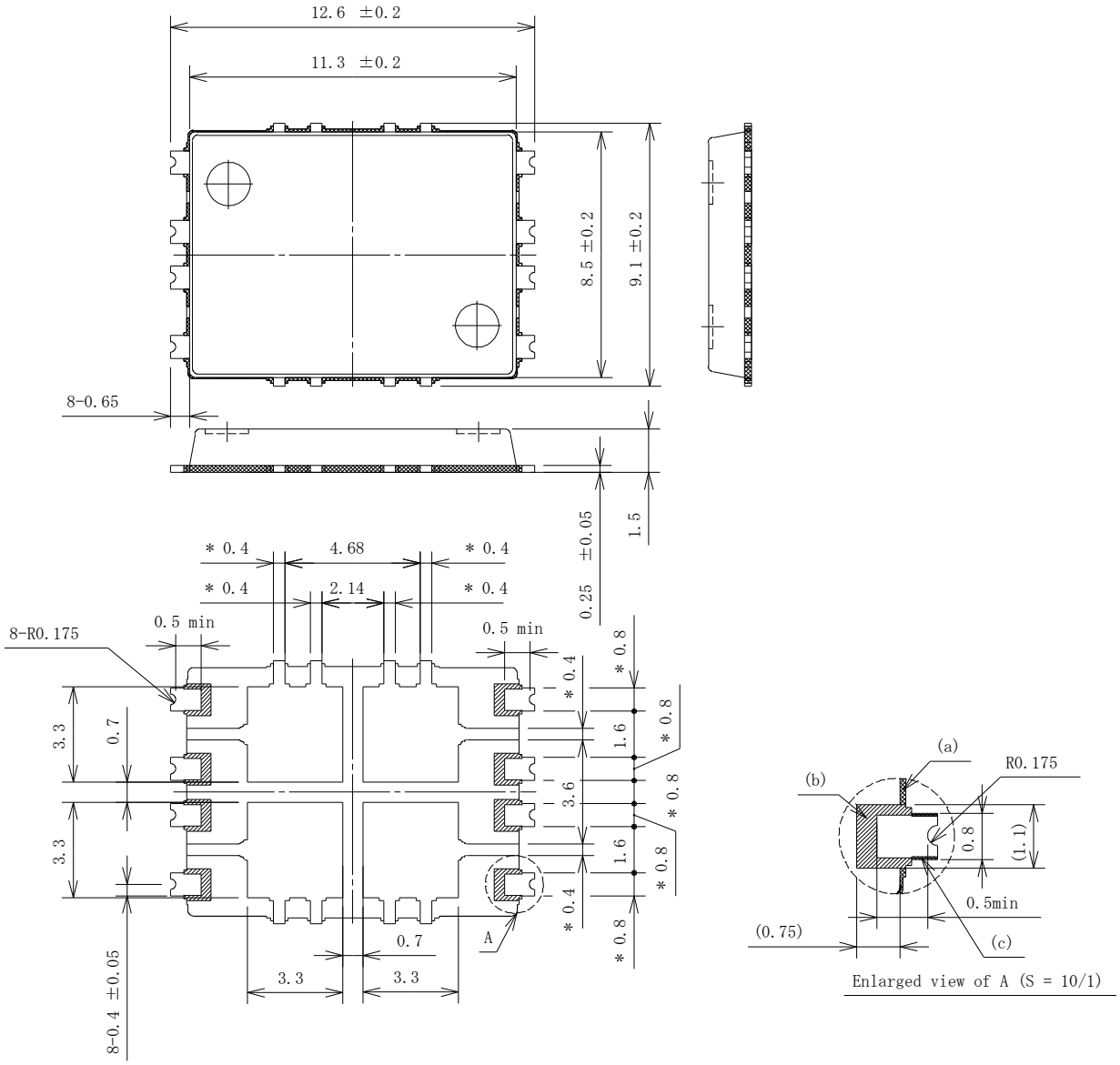




Pin Number	Description	Pin Number	Description
1	Q1 drain	11	Q3 drain
2	Q1 drain	12	Q3 drain
3	Q2 drain	13	Q4 drain
4	Q2 drain	14	Q4 drain
5	Q2 gate	15	Q4 gate
6	Q2 drain	16	Q4 drain
7	Q2 source	17	Q4 source
8	Q3 source	18	Q1 source
9	Q3 drain	19	Q1 drain
10	Q3 gate	20	Q1 gate

Physical Dimensions

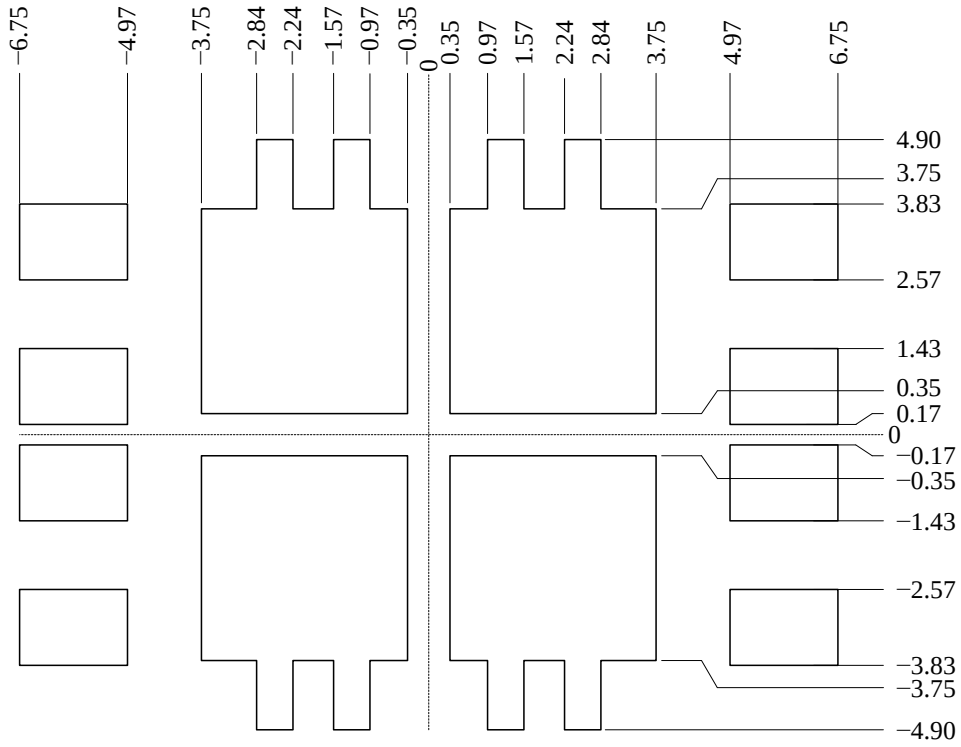
● **HSON-20 Package**



NOTES:

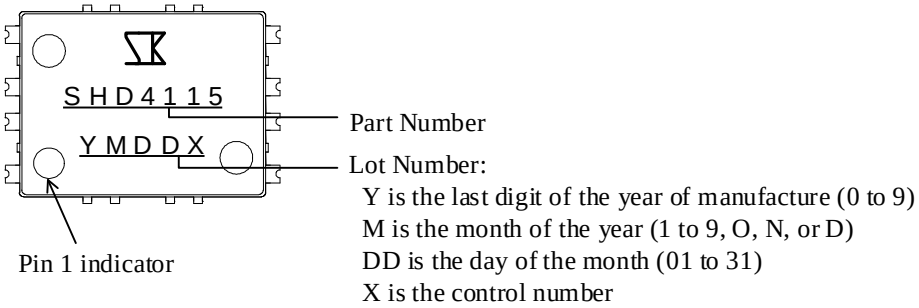
- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Dimensions without tolerances have a tolerance of ±0.1.
- Dimensions with the asterisks do not include any mold flash.
- (a) depicts the area where one or more mold flashes similar in thickness to that of the frame may exist.
- (b) depicts the area where a groove is formed with a target depth of 0.05.
- (c) depicts the area where a frame is crushed with a target width of 0.05.
- Moisture Sensitivity Level 3 (MSL 3)
- When soldering the products, it is required to minimize the working time within the following limits:
  Reflow
    Preheat: 150 °C to 200 °C / 60 s to 120 s
    Solder heating: 255 °C / 30s, 3 times (260 °C peak)
  Soldering iron: 350 °C / 3.5 s, 1 time
- The following pins are not guaranteed to be connected by soldering: 6, 9, 16, and 19.

● **HSON-20 Land Pattern Example**



Unit : mm

Marking Diagram



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DSGN-AEZ-16003