Off-Line PWM Controllers with Integrated Power MOSFET

STR3W400MXD Series

Data Sheet

Description

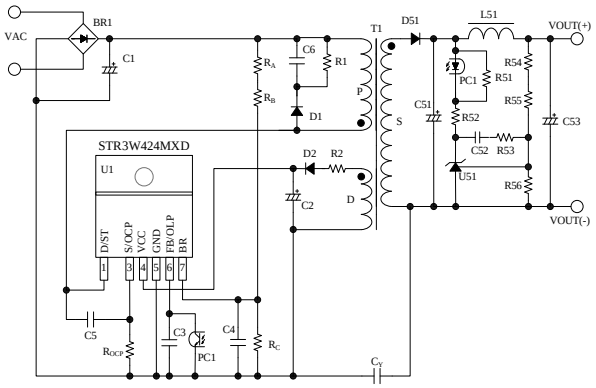
The STR3W400MXD series is power IC for switching power supplies, incorporating a power MOSFET and a current mode PWM controller IC.

The operating mode of the IC automatically changes to green-mode or burst oscillation mode according to load in order to improve the all load efficiency. The product achieves high cost-performance power supply systems with few external components.

Features

- Bare Lead Frame: Pb-free (RoHS Compliant)
- Current Mode Type PWM Control
- Improving circuit efficiency (Since the step drive control can keep V_{RM} of secondary rectification diodes low, the circuit efficiency can be improved by low V_F)
- Automatically changed operation mode in response to load conditions
  Fixed switching frequency mode, 65 kHz (typ.)
  Green mode, 30 kHz (typ.) to 65 kHz (typ.)
  Burst oscillation mode
- No Load Power Consumption, P_{IN} < 30 mW
- Soft Start Function
- Random Switching Function
- Slope Compensation Function
  (Subharmonic Oscillation Prevention)
- Leading Edge Blanking Function
- Bias Assist Function
- Protections
  – Two Types of Overcurrent Protection (OCP): Pulse-by-Pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
  – Overload Protection (OLP): Auto-restart
  – AC Input Voltage Detection Function
    Overvoltage Protection (HVP): Auto-restart
    Brown-In and Brown-Out Function: Auto-restart
  – Overvoltage Protection (OVP): Auto-restart
  – Thermal Shutdown (TSD): Auto-restart with hysteresis

Typical Application



Package

TO-220F-6L

Not to scale

Selection Guide

- Electrical Characteristics
  f_{OSC} = 65 kHz
  V_{DSS} (min.) = 700 V
- Power MOSFET On-resistance and Output Power, P_{OUT}*1

Products	$R_{DS(ON)}$ (max.)	P_{OUT}	
		230 VAC	85 to 265 VAC
STR3W422MXD*2	2.8 Ω	60 W	40 W
STR3W424MXD	1.1 Ω	110 W	70 W
STR3W426MXD*2	1.0 Ω	130 W	80 W

*1 The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, duty cycle, and thermal design affect the output power. It may be less than the value stated here.

*2 Under development

Applications

- White Goods
- Office Automation Equipment
- Industrial Equipment
- Other SMPS

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C

Characteristic	Symbol	Test Conditions	Pin	Rating	Units	Remarks
Drain Peak Current(1)	I_{DPEAK}	Single Pulse	1 − 3	TBD	A	STR3W422MXD
				10.6		STR3W424MXD
				TBD		STR3W426MXD
Maximum Switching Current(2)	I_{DMAX}	Single Pulse T_A = –40 to 115 °C	1 − 3	TBD	A	STR3W422MXD
				5.9		STR3W424MXD
				TBD		STR3W426MXD
Avalanche Energy(3)(4)	E_{AS}	TBD	1 – 3	TBD	mJ	STR3W422MXD
		I_{LPEAK} = 0.5 A		2.9		STR3W424MXD
		TBD		TBD		STR3W426MXD
D/ST Pin Voltage	$V_{D/ST}$		1 − 5	−1 to V_{DSS}	V	
S/OCP Pin Voltage	$V_{S/OCP}$		3 − 5	−2 to 6	V	
VCC Pin Voltage	V_{CC}		4 – 5	32	V	
FB/OLP Pin Voltage	V_{FB}	$I_{FB} \leq$ 1 mA	6 – 5	−0.3 to 14	V	
FB/OLP Pin Sink Current	I_{FB}		6 – 5	1.0	mA	
BR Pin Voltage	V_{BR}		7 – 5	−0.3 to 7	V	
BR Pin Sink Current	I_{BR}		7 – 5	1.0	mA	
Power Dissipation of Power MOSFET(5)	P_{D1}	With infinite heatsink	1 − 3	TBD	W	STR3W422MXD
				20.1		STR3W424MXD
				TBD		STR3W426MXD
		Without heatsink	1 − 3	TBD	W	
Power Dissipation of control Part	P_{D2}	Defined by $V_{CC} \times I_{CC}$	4 − 5	0.13	W	
Internal Frame Temperature in Operation	T_F		—	−40 to 115	°C	
Operating Ambient Temperature	T_{OP}		—	−40 to 115	°C	
Storage Temperature	T_{STG}		—	−40 to 125	°C	
Junction Temperature	T_J		—	150	°C	

(1) See Section 4.2.
(2) The maximum switching current is the drain current determined by the drive voltage of the IC and threshold voltage (V_{TH}) of the power MOSFET.
(3) See Figure 4-2.
(4) Single pulse, V_{DD} = 99 V, L = 20 mH
(5) See Section 4.3.

2. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 18 V

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		4 − 5	13.8	15.0	16.2	V	
Operation Stop Voltage(1)	$V_{CC(OFF)}$		4 − 5	7.6	8.5	9.2	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	4 − 5	—	1.7	3.0	mA	
Startup Circuit Operation Voltage	$V_{ST(ON)}$		1 − 5	40	47	55	V	
Startup Current	$I_{CC(ST)}$	V_{CC} = 13.5 V	4 − 5	−4.5	−2.5	−1.2	mA	
Startup Current Biasing Threshold Voltage	$V_{CC(BIAS)}$	I_{CC}=−500μA	4 − 5	8.0	9.6	10.5	V	
Normal Operation								
Average Switching Frequency	$f_{OSC(AVG)}$		1 − 5	58	65	72	kHz	
Switching Frequency Modulation Deviation	Δf		1 − 5	—	5.4	—	kHz	
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V	6 − 5	−240	−180	−120	μA	
Minimum Feedback Current	$I_{FB(MIN)}$		6 − 5	−21	−13	−5	μA	
Light Load Operation								
FB/OLP Pin Starting Voltage of Frequency Decreasing	$V_{FB(FDS)}$		6 − 5	1.68	2.15	2.51	V	
FB/OLP Pin Ending Voltage of Frequency Decreasing	$V_{FB(FDE)}$		6 − 5	1.42	1.77	2.11	V	
Minimum Switching Frequency	$f_{OSC(MIN)}$		1 − 5	23	30	37	kHz	
Standby Operation								
FB/OLP Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		6 − 5	1.02	1.12	1.22	V	
AC Input Voltage Detection Operation								
AC Input Overvoltage Protection (HVP) Threshold Voltage(2)	$V_{BR(HVP)}$		7 − 5	5.34	5.51	5.68	V	
AC Input Overvoltage Protection (HVP) Release Threshold Voltage	$V_{BR(HVPR)}$		7 − 5	5.23	5.39	5.55	V	
Brown-in Threshold Voltage	$V_{BR(IN)}$		7 − 5	1.02	1.11	1.2	V	
Brown-out Threshold Voltage	$V_{BR(OUT)}$		7 − 5	0.76	0.85	0.94	V	
Protection								
Maximum Duty Cycle	D_{MAX}		1 − 5	70	75	80	%	
Leading Edge Blanking Time	t_{BW}		—	—	330	—	ns	
OCP Compensation Coefficient	DPC		—	—	17.3	—	mV/μs	

(1) $V_{CC(BIAS)} > V_{CC(OFF)}$ always.
(2) $V_{BR(HVP)} > V_{BR(HVPR)}$

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
OCP Compensation Duty Cycle	D_{DPC}		—	—	36	—	%	
OCP Threshold Voltage at Zero Duty Cycle	$V_{OCP(L)}$		3 − 5	0.735	0.795	0.855	V	
OCP Threshold Voltage at 36% Duty Cycle	$V_{OCP(H)}$		3 − 5	0.843	0.888	0.933	V	
OCP Threshold Voltage During LEB (t_{BW})	$V_{OCP(LEB)}$		3 − 5	—	1.69	—	V	
OLP Threshold Voltage	$V_{FB(OLP)}$	V_{CC} = 32 V	6 − 5	6.8	7.3	7.8	V	
OLP Operation Current	$I_{CC(OLP)}$	V_{CC} = 12 V	4 − 5	—	260	—	µA	
OLP Delay Time	t_{OLP}		—	55	75	90	ms	
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		6 − 5	10.5	11.8	13.5	V	
OVP Threshold Voltage	$V_{CC(OVP)}$		4 − 5	27.0	29.1	31.2	V	
Thermal Shutdown Operating Temperature	$T_{J(TSD)}$		—	127	145	—	°C	
Thermal Shutdown Hysteresis Temperature	$T_{J(TSD)HYS}$		—	—	80	—	°C	
Power MOSFET								
Drain-to-Source Breakdown Voltage	V_{DSS}	I_{DS} = 300 µA	1 − 3	700	—	—	V	
Drain Leakage Current	I_{DSS}	V_{DS} = V_{DSS}	1 − 3	—	—	300	µA	
On-resistance	$R_{DS(ON)}$		1 − 3	—	—	2.8	Ω	STR3W422MXD
				—	—	1.4		STR3W424MXD
				—	—	1.0		STR3W426MXD
Switching Time	t_f		1 − 3	—	—	250	ns	
Thermal Resistance								
Junction to Frame Thermal Resistance[3]	θ_{J-F}		—	—	—	TBD	°C/W	STR3W422MXD
				—	—	3.4		STR3W424MXD
				—	—	TBD		STR3W426MXD

[3] θ_{J-F} is thermal resistance between junction of power MOSFET and frame. Frame temperature (T_F) is measured at the center of the case top surface.

3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	2.3	—	g
Heatsink Mounting Screw Torque		0.588	—	0.785	N·m

4. Performance Curves

4.1 Derating Curves

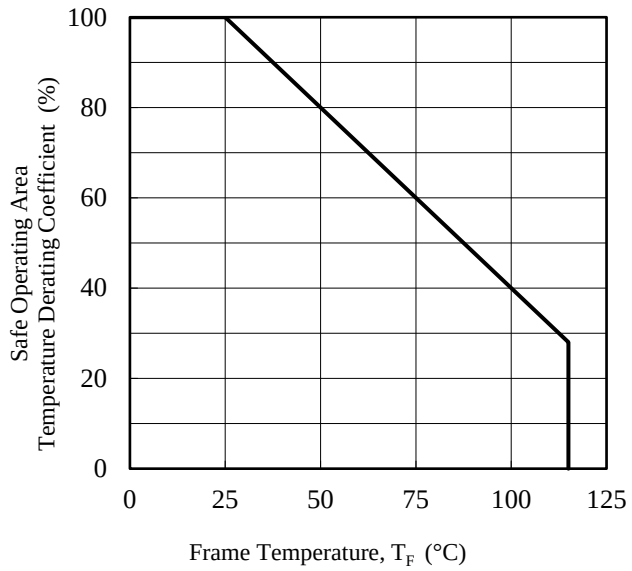


Figure 4-1. SOA Temperature Derating Coefficient Curve

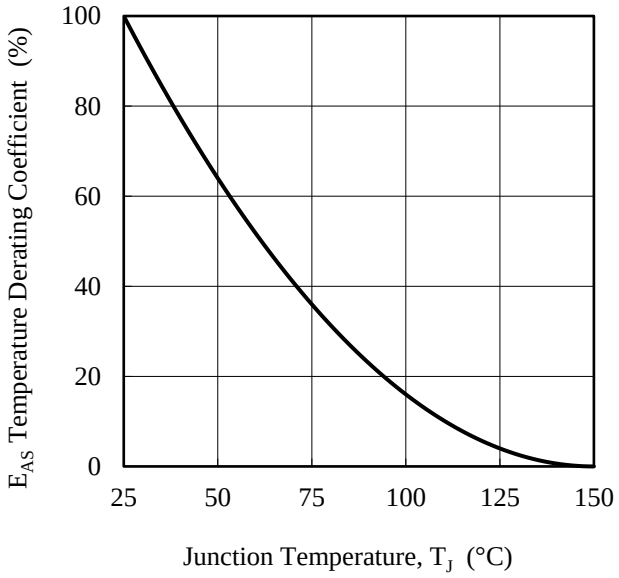


Figure 4-2. Avalanche Energy Derating Coefficient Curve

4.2 Power MOSFET Safe Operating Area Curves

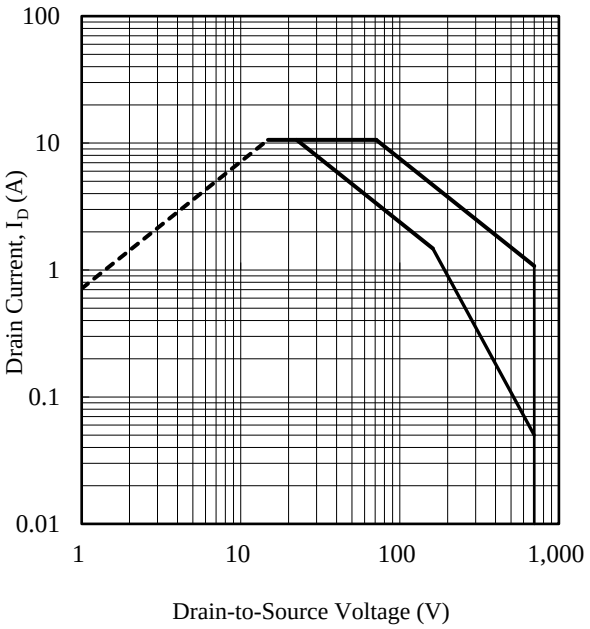
When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 4-1. The broken line in the safe operating area curve is the drain current curve limited by on-resistance.

Unless otherwise specified, T_A = 25 °C, Single pulse.

- **STR3W422MXD**

TBD

- **STR3W424MXD**



- **STR3W426MXD**

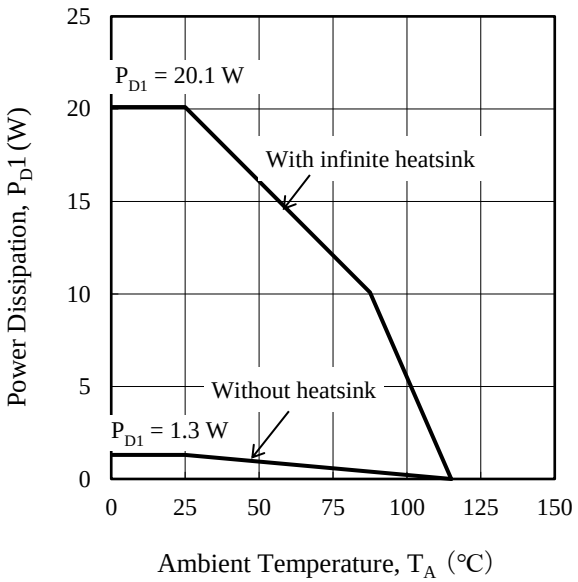
TBD

4.3 Ambient Temperature versus Power Dissipation Curves

• **STR3W422MXD**

TBD

• **STR3W424MXD**

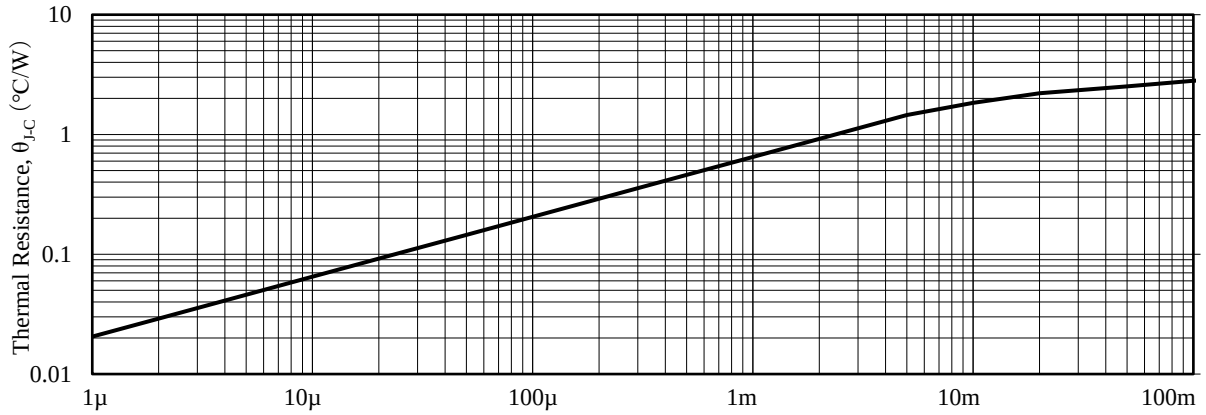


• **STR3W426MXD**

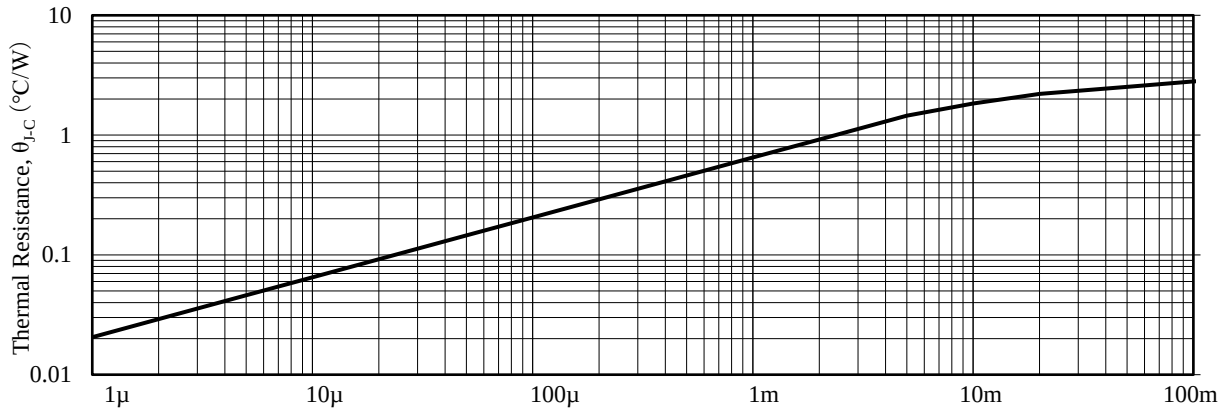
TBD

4.4 Transient Thermal Resistance Curves

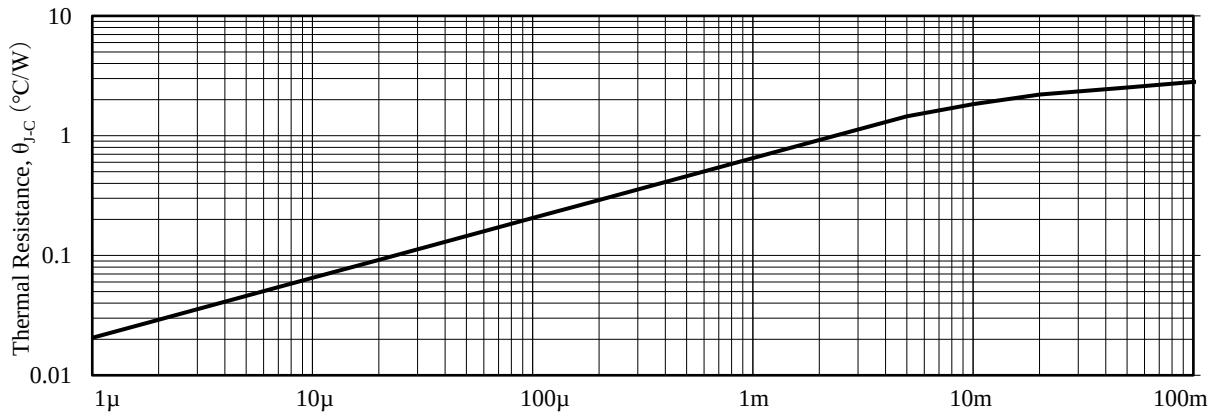
- **STR3W422MXD**



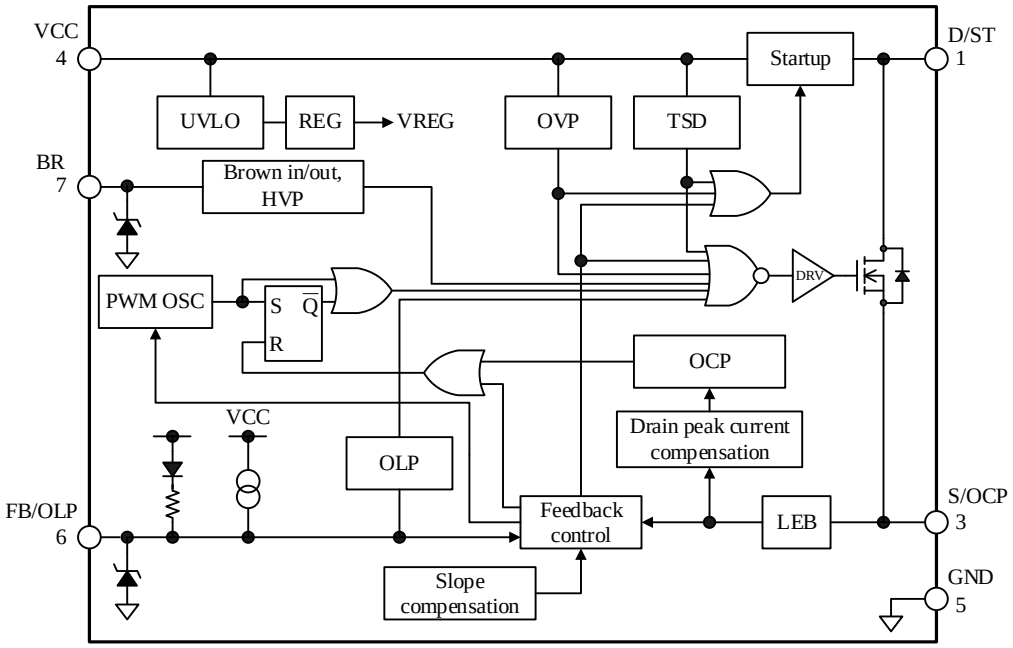
- **STR3W424MXD**



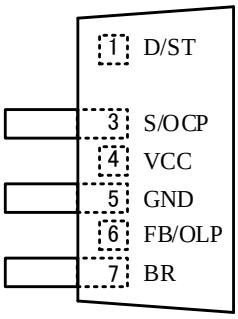
- **STR3W426MXD**



5. Block Diagram



6. Pin Configuration Definitions



(LF2012)

Pin	Name	Descriptions
1	D/ST	Power MOSFET Drain and input of the startup current
2	–	(Pin removed)
3	S/OCP	Power MOSFET Source ,input of current mode control signal and OCP signal
4	VCC	Power supply voltage input for the IC, and input of OVP signal
5	GND	Ground
6	FB/OLP	Feedback signal input for constant voltage control signal, and input of OLP signal
7	BR	AC input voltage detection signal input

7. Typical Application

The PCB traces D/ST pins should be as wide as possible, in order to enhance thermal dissipation.

In applications having a power supply specified such that V_{DS} has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

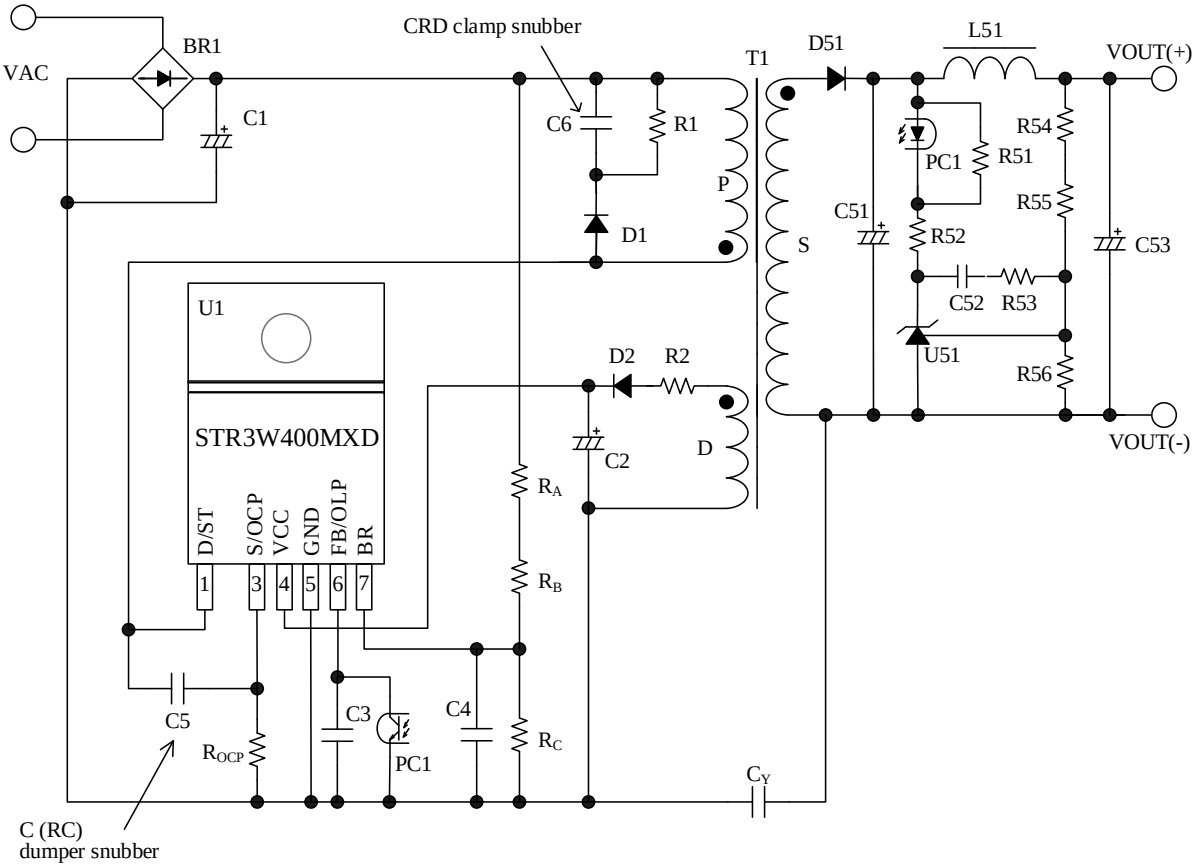
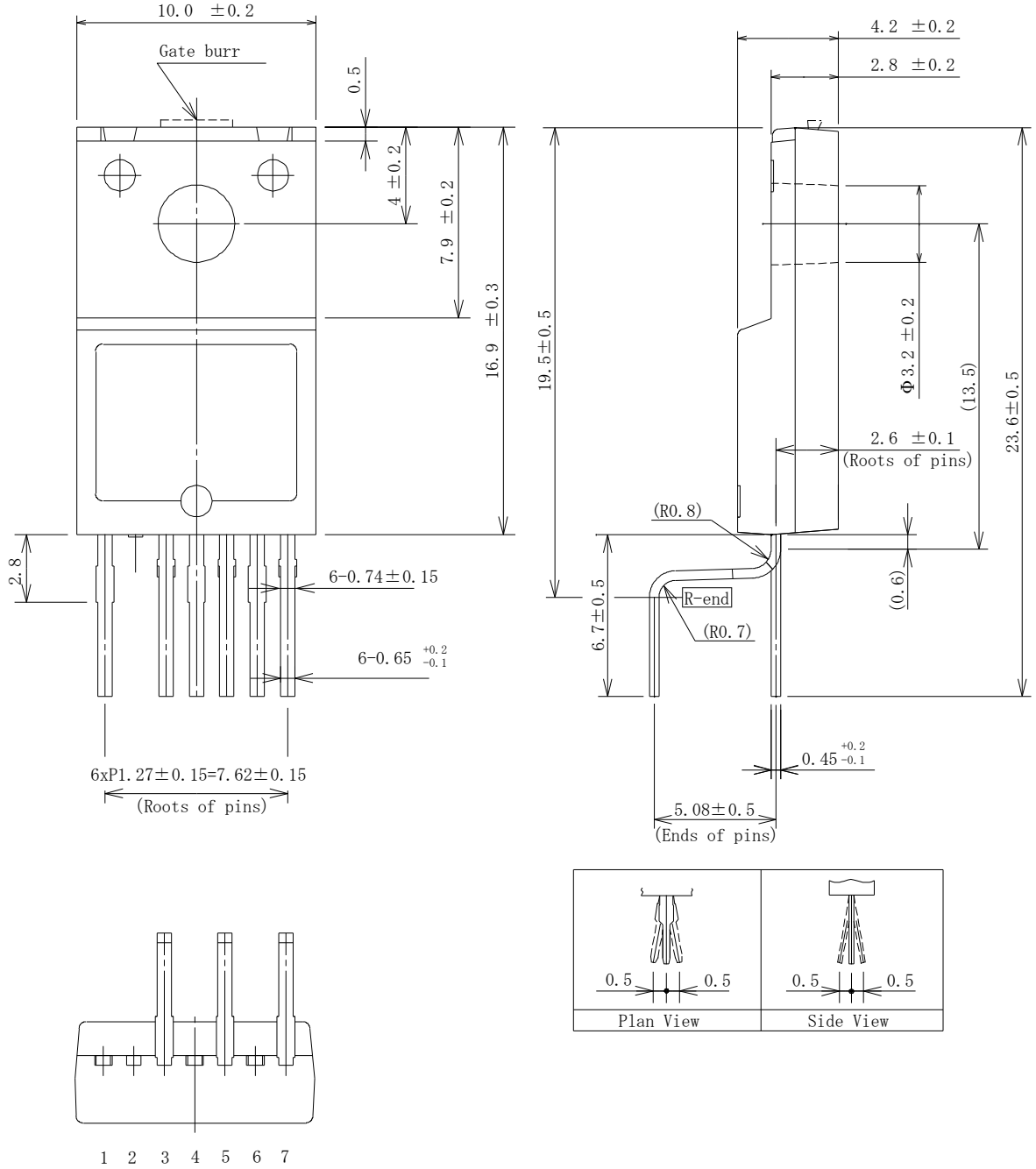


Figure 7-1. Typical Application

8. External Dimensions

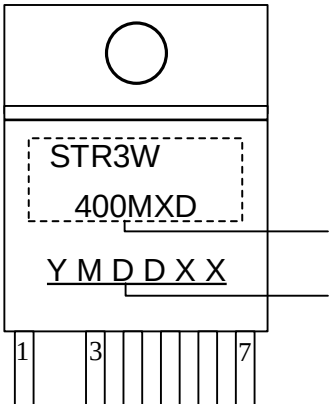
● TO-220F-6L (LF2012)



NOTES:

- Dimensions in millimeters
- "Gate burr" indicates protrusion of 0.3 mm (max.).
- Bare lead frame: Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 ± 5 °C / 10 ± 1 s, 2 times
  Soldering Iron: 380 ± 10 °C / 3.5 ± 0.5 s, 1 time
  Soldering should be at a distance of at least 1.5 mm from the body of the product.

9. Marking Diagram



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
DD is the day of the month (01 to 31)
XX is the control number

10. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

10.1 Startup Operation

Figure 10-1 shows the circuit around the VCC pin.

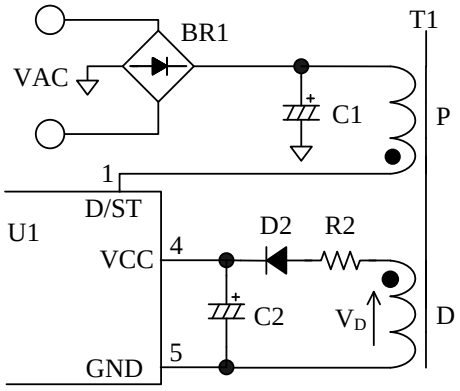


Figure 10-1. VCC Pin Peripheral Circuit

The IC incorporates the startup circuit. The circuit is connected to the D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{ST(ON)}$ = 47 V, the startup circuit starts operation. During the startup process, the constant current, $I_{CC(ST)}$ = −2.5 mA, charges C2 at the VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts switching operation. During the IC operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 10-1 becomes a power source to the VCC pin.

After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero. The approximate value of auxiliary winding voltage is about 18V, taking account of the winding turns of D winding so that the VCC pin voltage becomes Equation (1) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.})$$

$$\Rightarrow 10.5\ (\text{V}) < V_{CC} < 27.0\ (\text{V}) \qquad (1)$$

The startup time of the IC is determined by C2 capacitor value. The approximate startup time t_{START} is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left|I_{CC(ST)}\right|} \qquad (2)$$

where,

t_{START} : Startup time of the IC (s)

$V_{CC(INT)}$: Initial voltage on the VCC pin (V)

10.2 Undervoltage Lockout (UVLO)

Figure 10-2 shows the relationship of VCC pin voltage and circuit current I_{CC}. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

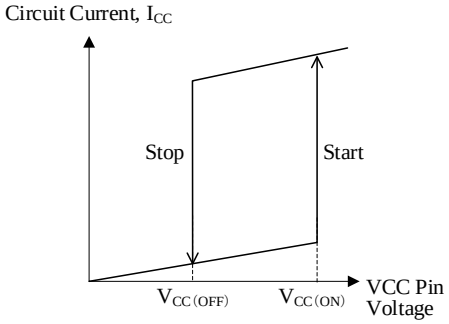


Figure 10-2. Relationship between VCC Pin Voltage and I_{CC}

10.3 Bias Assist Function

By the bias assist function, the startup failure is prevented.

When FB pin voltage is the FB/OLP Pin Oscillation Stop Threshold Voltage, $V_{FB(OFF)}$ or less and VCC pin voltage decreases to the Startup Current Biasing Threshold Voltage, $V_{CC(BIAS)}$ = 9.6 V, the bias assist function is activated.

When the bias assist function is activated, the VCC pin voltage is kept almost constant voltage, $V_{CC(BIAS)}$ by providing the startup current, $I_{CC(ST)}$, from the startup circuit. Thus, the VCC pin voltage is kept more than $V_{CC(OFF)}$.

Since the startup failure is prevented by the bias assist function, the value of C2 connected to the VCC pin can be small. Thus, the startup time and the response time of the overvoltage protection (OVP) become shorter.

The operation of the bias assist function in startup is as follows. It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

Figure 10-3 shows the VCC pin voltage behavior during

the startup period. After the VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V at startup, the IC starts the operation. Then circuit current increases and the VCC pin voltage decreases. At the same time, the auxiliary winding voltage, V_D, increases in proportion to output voltage. These are all balanced to produce the VCC pin voltage.

When the VCC pin voltage is decrease to $V_{CC(OFF)}$ = 8.5 V in startup operation, the IC stops switching operation and a startup failure occurs. When the output load is light at startup, the output voltage may become more than the target voltage due to the delay of feedback circuit. In this case, the FB pin voltage is decreased by the feedback control. When the FB pin voltage decreases to $V_{FB(OFF)}$ or less, the IC stops switching operation and the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated and the startup failure is prevented.

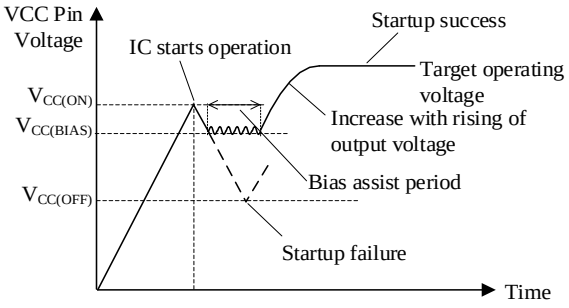


Figure 10-3. VCC Pin Voltage during Startup Period

10.4 Soft Start Function

Figure 10-4 shows the behavior of VCC pin voltage and drain current during the startup period.

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 8.75 ms. during the soft start period, overcurrent threshold is increased step-wisely (7 steps). This function reduces the voltage and the current stress of a power MOSFET and the secondary side rectifier diode.

Since the Leading Edge Blanking Function (see Section 10.6) is deactivated during the soft start period, there is the case that ON time is less than the leading edge blanking time, t_{BW} = 330 ns.

After the soft start period, D/ST pin current, I_D, is limited by the overcurrent protection (OCP), until the output voltage increases to the target operating voltage. This period is given as t_{LIM}.

In case t_{LIM} is longer than the OLP Delay Time, t_{OLP}, the output power is limited by the overload protection (OLP) operation.

Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the t_{LIM} is less than t_{OLP} = 55 ms (min.).

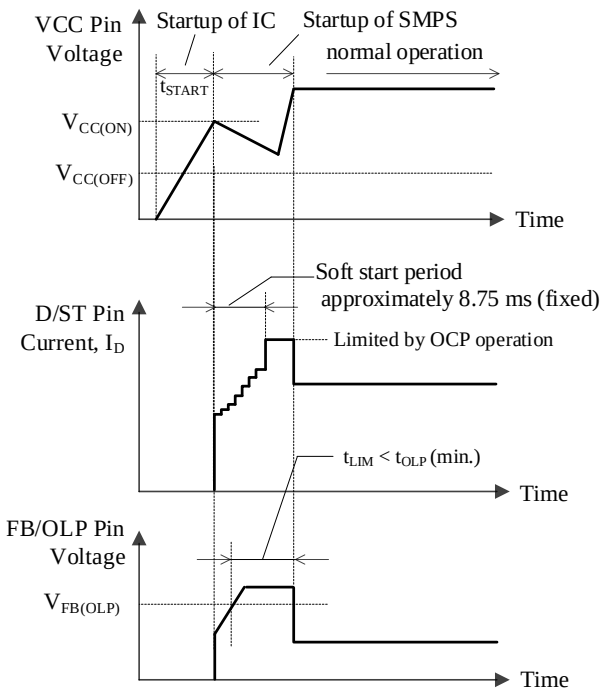


Figure 10-4. V_{CC} and I_D Waveforms during Startup

10.5 Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation. The FB/OLP pin voltage is internally added the slope compensation at the feedback control (see Section 5. Block Diagram), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure 10-5 and Figure 10-6.

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from

decreasing.

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 10-7. This is called the subharmonics phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation Function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the duty cycle gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

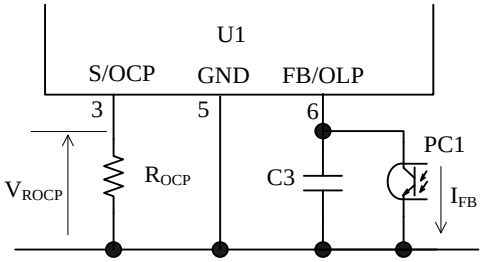


Figure 10-5. FB/OLP Pin Peripheral Circuit

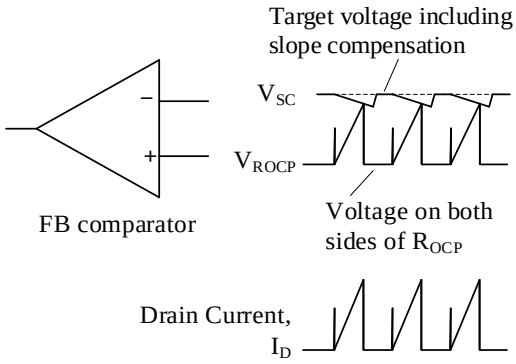


Figure 10-6. Drain Current, I_D, and FB Comparator Operation in Steady Operation

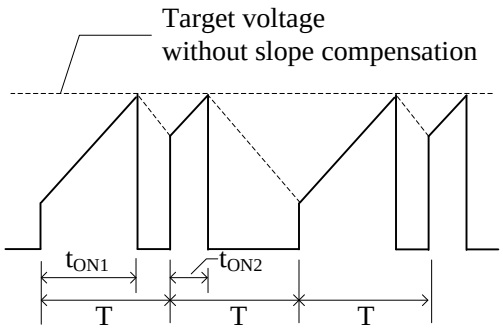


Figure 10-7. Drain Current, I_D, Waveform in Subharmonic Oscillation

10.6 Leading Edge Blanking Function

The constant voltage control of output of the IC uses the peak-current-mode control method.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of a FB comparator or overcurrent protection (OCP) circuit to the steep surge current in turning on a power MOSFET.

In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking, t_{BW} = 330 ns is built-in. During t_{BW}, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V in order not to respond to the turn-on drain current surge (see Section 10.10).

10.7 Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

10.8 Operation Mode

The IC has the function that automatically changes to the oscillation mode to green mode or burst oscillation mode (see Figure 10-8). The function reduces the switching loss and achieves higher efficiency at light load

When the output load becomes lower, FB/OLP pin voltage decreases. When the FB/OLP pin voltage decreases to $V_{FB(FDS)}$ = 2.15 V or less, the green mode is activated and the oscillation frequency starts decreasing. When the FB/OLP pin voltage becomes $V_{FB(FDE)}$ = 1.77 V, the oscillation frequency stops decreasing. At this point, the oscillation frequency becomes $f_{OSC(MIN)}$ = 30 kHz. When the FB/OLP pin voltage further decreases and becomes the standby operation point, the burst oscillation

mode is activated. As shown in Figure 10-9, the burst oscillation mode consists of the switching period and the non-switching period. The oscillation frequency during the switching period is the Minimum Frequency, $f_{OSC(MIN)}$ = 30 kHz.

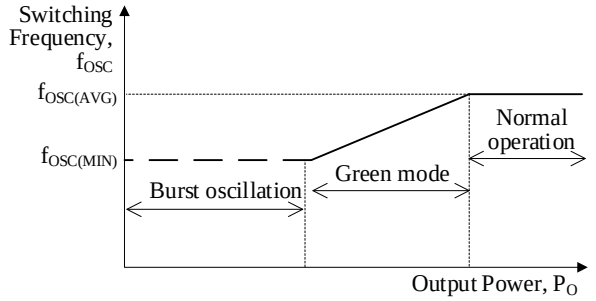


Figure 10-8. Relationship between P_O and f_{OSC}

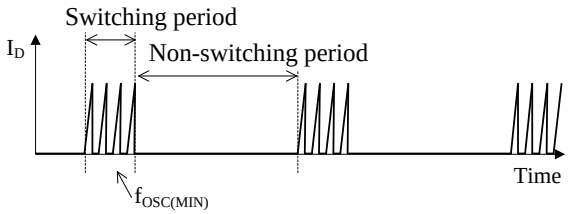


Figure 10-9. Switching Waveform at Burst Oscillation

Generally, in order to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst mode, audible noises can be reduced.

The IC has some detection delay time. The higher the AC input voltage is, the steeper the slope of the drain current, I_D is. Thus, the peak of I_D at automatic standby mode becomes high at a high AC input voltage.

It is necessary to consider that the burst frequency becomes low at a high AC input.

If VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.6 V during the transition to the burst mode, the bias assist function is activated and stabilizes the standby mode, because the Startup Current, $I_{CC(ST)}$, is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$. However, if the bias assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and the secondary-side winding and/or reducing the value of R2 in Figure 11-2 (see Section 11.1).

10.9 Step Drive Control

Figure 10-10 shows a flyback control circuit. The both end of secondary rectification diode (D51) is generated surge voltage when a power MOSFET turns on. Thus, V_{RM} of D51 should be set in consideration of the surge.

The IC optimally controls the gate drive of the internal power MOSFET (Step drive control) depending on the load condition. The step drive control reduces the surge voltage of D51 when the power MOSFET turns on (See Figure 10-11). Since V_{RM} of D51 can be set to lower value than usual, the price reduction and the increasing circuit efficiency are achieved by using a diode of low V_F.

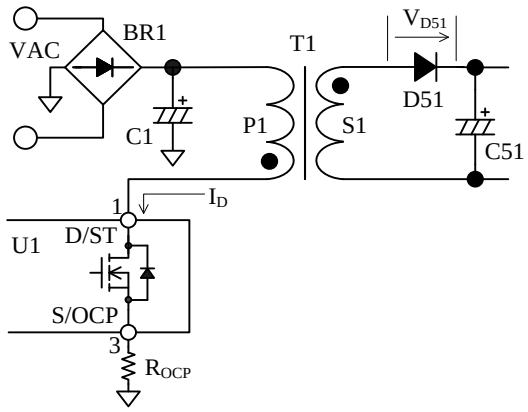


Figure 10-10. Flyback Control Circuit

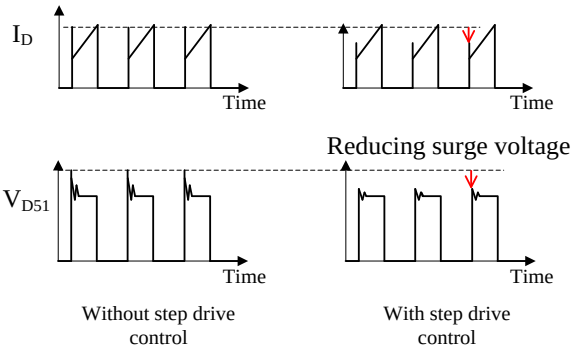


Figure 10-11. I_D and V_{D51} Waveforms

10.10 AC Input Voltage Detection Function

This function has the following:

- AC Input Overvoltage Protection (HVP)
- Brown-In and Brown-Out Function

This function turns on and off switching operation according to the BR pin voltage detecting the AC input voltage, and thus prevents excessive input current and over heating.

Section 10.10.1 shows HVP, Section 10.10.2 shows Brown-In and Brown-Out Function. Figure 10-12 shows waveforms of the BR pin voltage and the drain currnet.

There are two types of detection method as shown in Section 10.10.3 and Section 10.10.4.

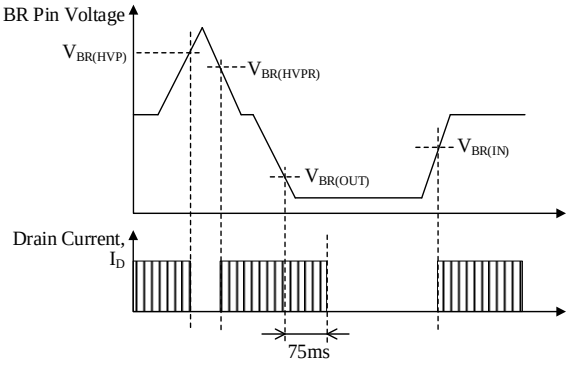


Figure 10-12. BR Pin Voltage and Drain Current Waveforms

10.10.1 AC Input Overvoltage Protection (HVP)

When the AC input voltage increases from steady state and the BR pin voltage reaches $V_{BR(HVP)}$ = 5.51 V or more, the IC stops switching operation.

After that, when the AC input voltage decreases and the BR pin voltage falls to $V_{BR(HVPR)}$ = 5.39 V or less, the IC starts switching operation.

By the hysteresis of the HVP threshold voltage, the HVP operation can keep stable without the response of small voltage fluctuations at the BR pin.

The function is disabled during switching operation stop in burst oscillation mode.

10.10.2 Brown-In and Brown-Out Function

Even if the IC is in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, when the AC input voltage decreases from steady-state and the BR pin voltage falls to $V_{BR(OUT)}$ = 0.85 V or less for the OLP Delay Time, t_{OLP} = 75 ms, the IC stops switching operation.

When the AC input voltage increases and the BR pin voltage reaches $V_{BR(IN)}$ = 1.11 V or more in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, the IC starts switching operation.

The function is disabled during switching operation stop in burst oscillation mode. When the BR pin voltage falls to $V_{BR(OUT)}$ or less in burst oscillation mode and the sum of switching operation period becomes t_{OLP} or more, the IC stops switching operation.

10.10.3 DC Line Detection

Figure 10-13 shows BR pin peripheral circuit of DC line detection. There is a ripple voltage on C1 occurring at a half period of AC cycle. In order to detect each peak of the ripple voltage, the time constant of R_C and C4 should be shorter than a half period of AC cycle.

Since the period of the ripple voltage is shorter than t_{OLP}, the switching operation does not stop when only the bottom part of the ripple voltage becomes lower than $V_{BR(OUT)}$.

Thus it minimizes the influence of load conditions on the voltage detection.

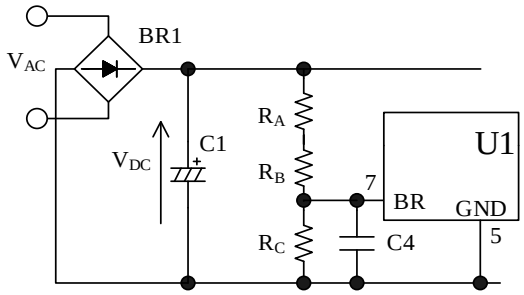


Figure 10-13. DC Line Detection

The components around BR pin:

- R_A and RB are a few megohms. Because of high voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
- R_C is a few hundred kilohms
- C4 is 470 pF to 2200 pF for high frequency noise rejection

Neglecting the effect of both input resistance and forward voltage of rectifier diode, the reference value of C1 voltage when HVP and Brown-In and Brown-Out Function is activated is calculated as follows:

$$V_{DC(OP)} = V_{BR(TH)} \times \left(1 + \frac{R_A + R_B}{R_C}\right) \quad (3)$$

where,

$V_{DC(OP)}$: C1 voltage when HVP and Brown-In and Brown-Out Function is activated

$V_{BR(TH)}$: Any one of threshold voltage of BR pin (see Table 10-1)

Table 10-1. BR Pin Threshold Voltage

Parameter	Symbol	Value (Typ.)
AC Input Overvoltage Protection (HVP) Threshold Voltage	$V_{BR(HVP)}$	5.51 V
AC Input Overvoltage Protection (HVP) Release Threshold Voltage	$V_{BR(HVPR)}$	5.39 V
Brown-In Threshold Voltage	$V_{BR(IN)}$	1.11 V
Brown-Out Threshold Voltage	$V_{BR(OUT)}$	0.85 V

$V_{DC(OP)}$ can be expressed as the effective value of AC input voltage using Equation (4).

$$V_{AC(OP)RMS} = \frac{1}{\sqrt{2}} + V_{DC(OP)} \quad (4)$$

R_A, R_B, R_C and C4 should be selected based on actual operation in the application.

10.10.4 AC Line Detection

Figure 10-14 shows BR pin peripheral circuit of AC line detection. In order to detect the AC input voltage, the time constant of R_C and C4 should be longer than the period of AC cycle. Thus the response of BR pin detection becomes slow compared with the DC line detection.

This method detects the AC input voltage, and thus it minimizes the influence from load conditions. Also, this method is free of influence from C1 charging and discharging time.

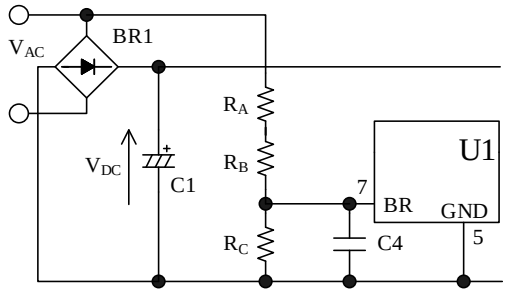


Figure 10-14. AC Line Detection

The components around BR pin:

- R_A and R_B are a few megohms. Because of high voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
- RC is a few hundred kilohms
- C4 is 0.22 µF to 1 µF for averaging AC input voltage and high frequency noise reduction. Rejection

Neglecting the effect of input resistance is zero, the reference effective value of AC input voltage when HVP and Brown-In and Brown-Out Function is activated is calculated as follows:

$$V_{AC(OP)RMS} = \frac{\pi}{\sqrt{2}} + V_{BR(TH)} \times \left(1 + \frac{R_A + R_B}{R_C}\right) \quad (5)$$

where,

$V_{AC(OP)RMS}$: The effective value of AC input voltage when HVP and Brown-In and Brown-Out Function is activated

$V_{BR(TH)}$: Any one of threshold voltage of BR pin (see Table 10-1)

R_A, R_B, R_C, and C4 should be selected based on actual operation in the application.

10.11 Overcurrent Protection (OCP)

10.11.1 OCP Operation

The overcurrent protection (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage.

During Leading Edge Blanking Time, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V which is higher than the normal OCP threshold voltage as shown in Figure 10-15. Changing to this threshold voltage prevents the IC from responding to the surge voltage in turning-on the power MOSFET. This function operates as protection at the condition such as output windings shorted or unusual withstand voltage of secondary-side rectifier diodes.

When the power MOSFET turns on, the surge voltage width of the S/OCP pin should be less than t_{BW}, as shown in Figure 10-15. In order to prevent surge voltage, pay extra attention to R_{OCP} trace layout (see Section 11.2). In addition, if a C (RC) damper snubber of Figure 10-16 is used, reduce the capacitor value of damper snubber.

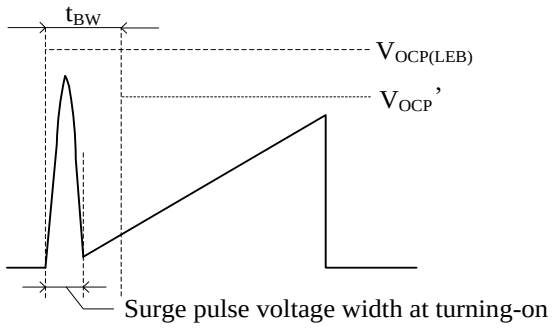


Figure 10-15. S/OCP Pin Voltage

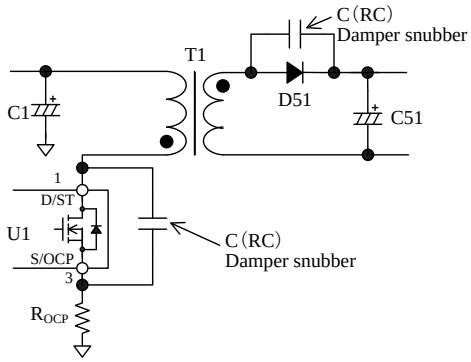


Figure 10-16. Damper Snubber

10.11.2 OCP Input Compensation Function

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to V_{OCP}. Thus, the peak current has some variation depending on AC input voltage in OCP state. In order to reduce the variation of peak current in OCP state, the IC has Input Compensation Function.

This function corrects OCP threshold voltage depending on the AC input voltage, as shown in Figure 10-17.

When the AC input voltage is low (Duty cycle is broad), the OCP threshold voltage is controlled to become high. The difference of peak drain current become small compared with the case where the AC input voltage is high (duty cycle is narrow).

The compensation signal depends on duty cycle. The relation between the duty cycle and the OCP threshold voltage after compensation V_{OCP}' is expressed as Equation (6). When duty cycle is broader than 36 %, the V_{OCP}' becomes a constant value $V_{OCP(H)}$ = 0.888 V

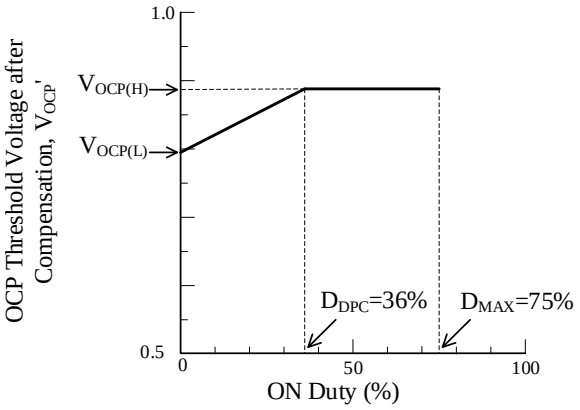


Figure 10-17. Relationship between Dduty Cycle and Drain Current Limit after Compensation

$$V_{OCP}' = V_{OCP(L)} + DPC \times ONTime$$

$$= V_{OCP(L)} + DPC \times \frac{Duty}{f_{OSC(AVG)}} \quad (6)$$

where,
$V_{OCP(L)}$: OCP Threshold Voltage at Zero Duty Cycle (V)
DPC: OCP Compensation Coefficient (mV/μs)
ONTime: On-time of power MOSFET (μs)
Duty: Duty cycle of power MOSFET (%)
$f_{OSC(AVG)}$: Average PWM Switching Frequency (kHz)

10.11.3 Overload Protection (OLP)

Figure 10-18 shows the FB/OLP pin peripheral circuit, and Figure 10-19 shows each waveform for overload protection (OLP) operation.

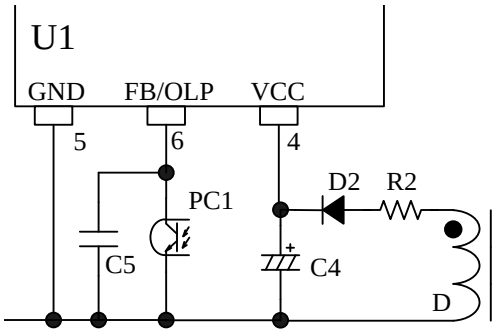


Figure 10-18. FB/OLP Pin Peripheral Circuit

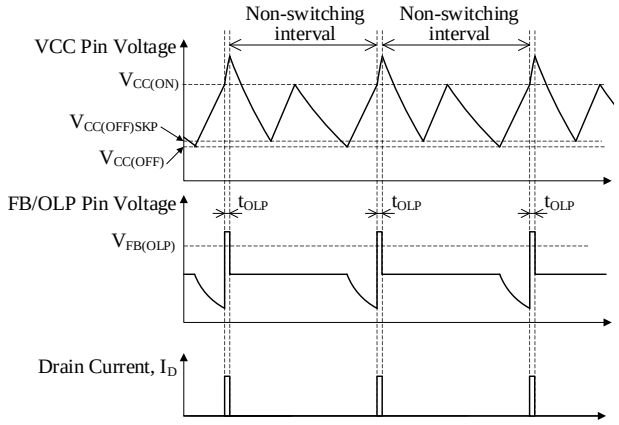


Figure 10-19. OLP Operational Waveforms

When the peak drain current of I_D is limited by the overcurrent protection operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C5 connected to the FB/OLP pin and FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 7.3 V or more for the OLP delay time, t_{OLP} = 75 ms or more, the OLP is activated, the IC stops switching operation.

During OLP operation, the intermittent operation by VCC pin voltage repeats and reduces the stress of parts such as a power MOSFET and secondary side rectifier diodes.

When the OLP is activated, the IC stops switching operation, and the VCC pin voltage decreases.

During OLP operation, the Bias assist function is disabled. When the VCC pin voltage decreases to $V_{CC(OFF)SKP}$ (about 9 V), the startup current flows, and the VCC pin voltage increases. When the VCC pin voltage increases to $V_{CC(ON)}$, the IC starts operation, and the circuit current increases. After that, the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V, the control circuit stops operation.

Skipping the UVLO operation of $V_{CC(OFF)}$ (see Section 10.2), the intermittent operation makes the non-switching interval longer and restricts the temperature rise of the power MOSFET.

When the abnormal condition is removed, the IC returns to normal operation automatically.

10.11.4 Overvoltage Protection (OVP)

Figure 10-20 shows the overvoltage protection (OVP) operational waveforms.

When a voltage between the VCC pin and the GND pin increases to $V_{CC(OVP)}$ = 29.1 V or more, OVP is activated and the IC stops switching operation. Since the Bias assist function is disabled during OVP operation, the VCC pin voltage decreases. When the VCC pin voltage becomes $V_{CC(OFF)}$, the IC stops operation and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$, and the IC starts switching operation again. In this way, the intermittent operation by the UVLO is repeated during the OVP operation.

When the fault condition is removed, the IC returns to normal operation automatically.

When VCC pin voltage is provided by using auxiliary winding of transformer, the VCC pin voltage is proportional to output voltage. Thus, the VCC pin can detect the overvoltage conditions such as output voltage detection circuit open. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (7).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.1 \text{ (V)} \quad (7)$$

where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

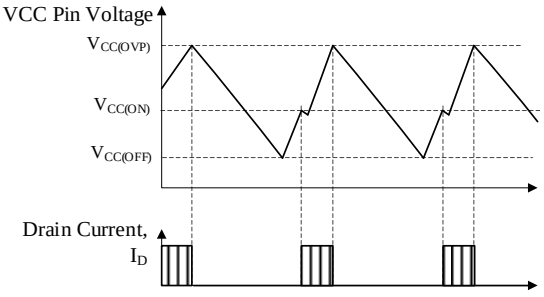


Figure 10-20. OVP Operational Waveforms

10.11.5 Thermal Shutdown (TSD)

Figure 10-21 shows the Thermal Shutdown (TSD) operational waveforms.

When the temperature of control circuit increases to $T_{J(TSD)}$ = 145 °C or more, TSD is activated, and the IC stops switching operation. After that, VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias assist function is activated and the VCC pin voltage is kept to over the $V_{CC(OFF)}$.

This type has the thermal hysteresis of TSD. When the temperature reduces to less than $T_{J(TSD)}$–$T_{J(TSD)HYS}$, the Bias Assist Function is disabled and the VCC pin voltage decreases. When the VCC pin voltage becomes $V_{CC(OFF)}$, the IC stops operation and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$, and the IC starts switching operation again. In this way, the intermittent operation by the TSD and the UVLO is repeated during an excess thermal condition.

When the fault condition is removed, the IC returns to normal operation automatically.

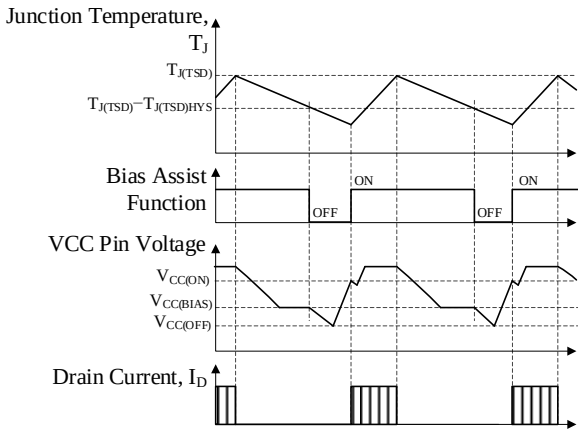


Figure 10-21. TSD Operational Waveforms

11. Design Notes

11.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

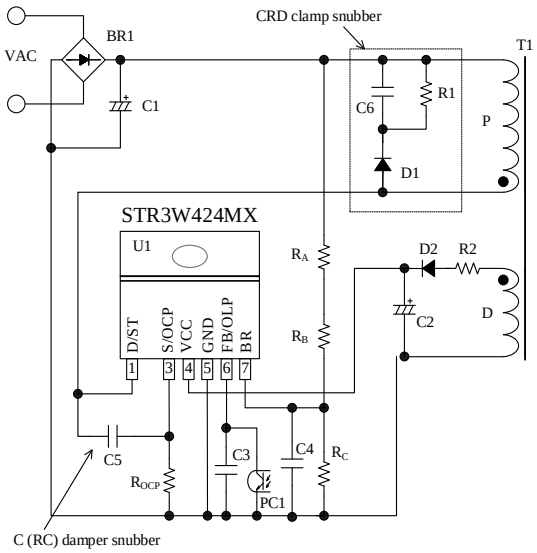


Figure 11-1. IC Peripheral Circuit

11.1.1 Input and Output Electrolytic Capacitor

Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

11.1.2 S/OCP Pin Peripheral Circuit

In Figure 11-1, R_{OCP} is the resistor for the current detection. Since high frequency switching current flows to R_{OCP}, choose the resistor of low inductance and high power dissipation capability.

11.1.3 VCC Pin Peripheral Circuit

The value of C2 in Figure 11-1 is generally recommended to be 10 µF to 47 µF (see Section 10.1 Startup Operation, because the startup time is determined by the value of C2)

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 11-2), and the overvoltage protection (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off. For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 11-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

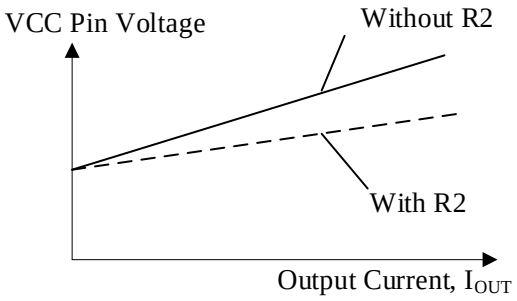


Figure 11-2. Variation of VCC Pin Voltage and Power

11.1.4 FB/OLP Pin Peripheral Circuit

C3 (see Figure 11-1) is for high frequency noise rejection and phase compensation, and should be connected close to the FB/OLP pin and the GND pin. The value of C3 is recommended to be about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

11.1.5 Snubber Circuit

In case the serge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 11-1);

- A clamp snubber circuit of a capacitor-resistor- diode (CRD) combination should be added on the primary winding P.
- A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.
  In case the damper snubber circuit is added, this components should be connected near D/ST pin and S/OCP pin.

11.1.6 Peripheral Circuit of Secondary-side Shunt Regulator

Figure 11-3 shows the secondary-side detection circuit with the standard shunt regulator IC (U51).

C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047 µF to 0.47 µF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

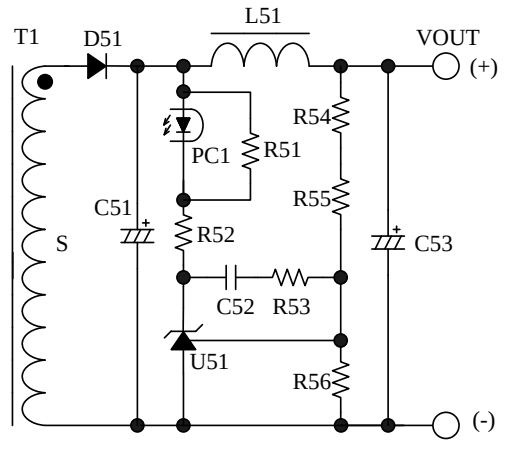


Figure 11-3. Peripheral Circuit of Secondary-side Shunt Regulator (U51)

11.1.7 Transformer

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the overvoltage protection (OVP) may be activated. In transformer design, the following should be considered;

- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3···) should be maximized to improve the line-regulation of those outputs

Figure 11-4 shows the winding structural examples of two outputs.

- Winding structural example (a):
  S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2. D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

- Winding structural example (b)
  P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.。
  D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.

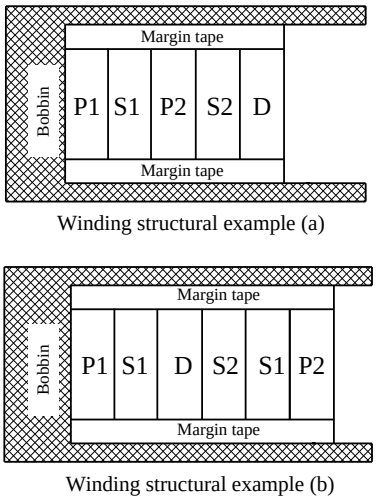


Figure 11-4. Winding Structural Examples

11.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace. In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 11-5 shows the circuit design example.

(1) Main Circuit
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.
If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground
Since the operation of the IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 11-5 as close to the R_{OCP} pin as possible.

(3) VCC Pin:
This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the GND pin is recommended.

(4) Current Detection Resistor, R_{OCP}:
R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 11-5) which is close to the base of R_{OCP}.

(5) Peripheral Components of the IC
Components of control circuit connected to the IC should be placed near the IC, and connected to the corresponding pin of the IC with a minimal length of traces.

(6) Secondary Rectifier Smoothing Circuit:
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations:
Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.
Since the copper area under the IC and the D/ST pin trace act as a heatsink, its traces should be as wide as possible.

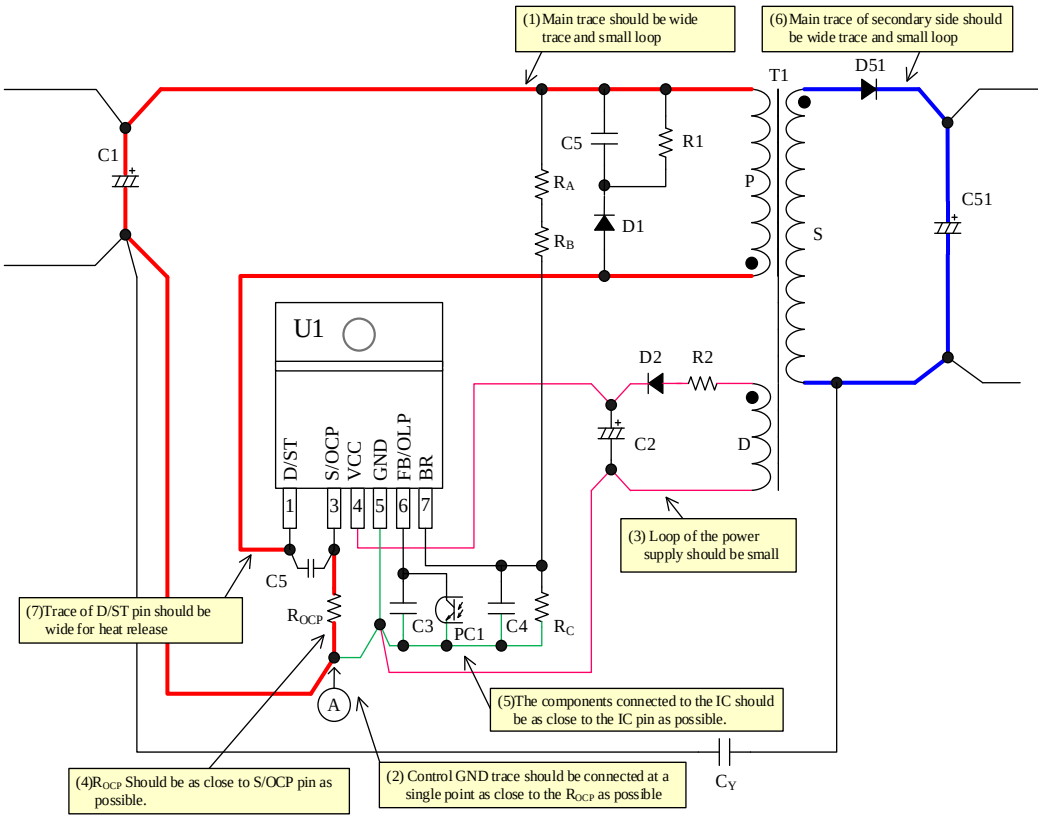


Figure 11-5. Peripheral Circuit Example Around IC

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