For Non-Isolated
Off-Line PWM Controllers with Integrated Power MOSFET

STR5A464x Series

Data Sheet

Description

The STR5A464x Series is power ICs for switching power supplies, incorporating a MOSFET and a current mode PWM controller IC for non-isolated Buck converter and Inverting converter topologies.

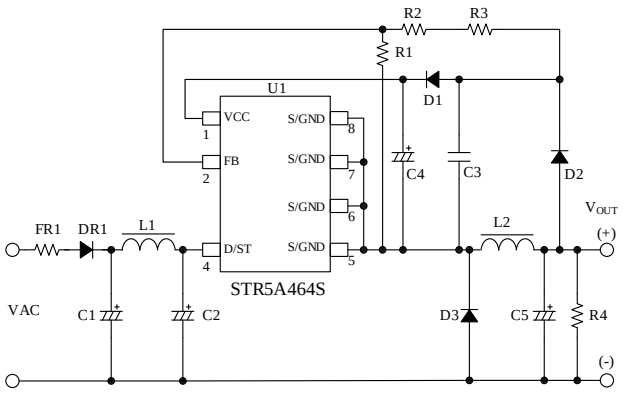
The operation mode is automatically changed, in response to load, to the fixed switching frequency, to the switching frequency control, and to the burst oscillation mode. Thus the power efficiency is improved.

The product achieves high cost-performance power supply systems with few external components.

Features

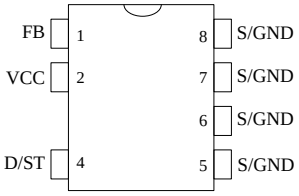
- Pb-free (RoHS compliant)
- Buck Converter
- Inverting Converter
- Current Mode PWM Control
- Automatically Switch the Operation Mode According to the Load
  Heavy Load: 60 kHz (typ.) Fixed Switching Frequency Mode
  Medium Load: Green Mode, 23 kHz (typ.) to 60 kHz (typ.)
  Light Load: Burst Oscillation Mode
- No Current Detection Resistor Required (Built-in Current Sensing MOSFET)
- Built-in Startup Function
- Built-in Error Amplifier
- Random Switching Function
- Leading Edge Blanking Function
- Soft Start Function
- Protections
  Overload Protection (OLP): Auto-restart
  Overvoltage Protection (OVP): Auto-restart
  Thermal Shutdown with Hysteresis (TSD): Auto-restart

Typical Application (Buck Convertor, STR5A464S)

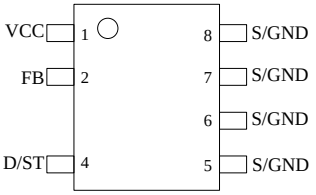


Package

DIP8



SOIC8



Not to scale

Selection Guide

- Electrical Characteristics
  $f_{OSC(AVG)}$ = 60 kHz (typ.)
  $V_{D/ST}$ = 700V (max.)

Part Number	$R_{DS(ON)}$ (max.)	I_{DLIM} (typ.)	Package
STR5A464D	13.6 Ω	0.41 A	DIP8
STR5A464S			SOIC8

Recommended Operating Condition

	Buck Converter	Inverting Converter
Input Voltage	AC 85 V to AC 265 V	
D/ST Input Voltage	≥ 40 V	
Output Voltage Range*	> 11 V < 27.5 V	> – 27.5 V < – 11 V

*Add a zener diode or a regulator to VCC pin when target output voltage is high.

Applications

- White Goods
- Auxiliary Power Supply
  (lighting Equipment with Microcomputer, etc.)
- Power Supply for Motor Control (actuator, etc.)
- Telecommunication Equipment
  (Convertible from 48 VDC to 15 VDC)
- Other SMPS

Contents

1. Absolute Maximum Ratings

The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC. Unless otherwise specified, T_A = 25 °C, all S/GND pins (5 pin to 8pin) are shorted.

The pin number of SOIC8 package products is shown in bracket.

Parameter	Symbol	Test Conditions	Pins	Rating	Units	Remarks
FB Pin Voltage	V_{FB}		1 – 5 (2 – 5)	− 0.3 to 7	V	
VCC Pin Voltage	V_{CC}		2 – 5 (1 – 5)	−0.3 to 32	V	
D/ST Pin Voltage	$V_{D/ST}$		4 – 5	−0.3 to 700	V	
Drain Peak Current	I_{DP}	Single pulse, Within 500 ns pulse width, $V_{D/ST} \leq 400$ V	4 – 5	1.7	A	
Maximum Switching Current[1]	I_{DMAX}	Negative: Within 2 µs pulse width	4 – 5	−0.2 to 0.97	A	STR5A464D
				−0.2 to 0.91		STR5A464S
MOSFET Power Dissipation	P_{D1}	[2]	—	1.55	W	STR5A464D
				1.51		STR5A464S
Operating Ambient Temperature	T_{OP}		—	−40 to 125	°C	
Storage Temperature	T_{STG}		—	−40 to 125	°C	
Junction Temperature	T_J		—	150	°C	

[1] See MOS FET Ta-P_D curve.

[2] When embedding this hybrid IC onto the printed circuit board (cupper area in a 15mm × 15mm)

2. Electrical Characteristics

The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC. Unless otherwise specified, T_A = 25 °C, all S/GND pins (5 pin to 8pin) are shorted.

The pin number of SOIC8 package products is shown in bracket.

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Remarks
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		2 – 5 (1 – 5)	13.6	15.0	16.6	V	
Operation Stop Voltage	$V_{CC(OFF)}$		2 – 5 (1 – 5)	7.3	8.0	8.7	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	2 – 5 (1 – 5)	—	—	2.0	mA	
Startup Circuit Operation Voltage	$V_{ST(ON)}$	V_{CC} = 13.5 V	4 – 5	19	29	39	V	
Startup Current	$I_{CC(ST)}$	V_{CC} = 13.5 V $V_{D/ST}$ = 100 V	2 – 5 (1 – 5)	−2.7	−1.5	−0.5	mA	
PWM Operation								
Average PWM Switching Frequency	$f_{OSC(AVG)}$	V_{FB}= 2.44 V	4 – 5	53	60	67	kHz	
Switching Frequency Modulation Deviation	Δf		4 – 5	—	2.8	—	kHz	
Feedback Reference Voltage	$V_{FB(REF)}$		1 – 5 (2 – 5)	2.44	2.50	2.56	V	
Feedback Current(1)	$I_{FB(OP)}$	V_{FB} = 2.3 V	1 – 5 (2 – 5)	−2.4	−0.8	—	µA	
Minimum Sampling Time	t_{FBMS}		1 – 5 (2 – 5)	—	—	2.5	µs	
Standby Drain Current	I_{DSTB}		4 – 5	—	50	—	mA	
Standby Operation Cycle	t_{STBOP}		4 – 5	530	740	940	µs	
Maximum ON Duty	D_{MAX}		4 – 5	50	57	64	%	
Protection								
Leading Edge Blanking Time(1)	t_{BW}		—	—	230	—	ns	
Drain Current Limit	I_{DLIM}		4 – 5	0.37	0.41	0.45	A	
OVP Threshold Voltage	$V_{CC(OVP)}$		2 – 5 (1 – 5)	27.5	29.3	31.3	V	
OLP Delay Time at Startup	t_{OLP}	V_{FB}= 0 V	4 – 5	—	72	—	ms	
Standby Blanking Time at Startup	$t_{STB(INH)}$	V_{FB}= 2.6 V	4 – 5	3.5	5.2	6.8	ms	
Thermal Shutdown Operating Temperature(1)	$T_{J(TSD)}$		—	135	—	—	°C	
Thermal Shutdown Hysteresis(1)	$T_{J(TSD)HYS}$		—	—	70	—	°C	
Power MOSFET								
Drain Leakage Current(1)	I_{DSS}	T_J = 125 °C $V_{D/ST}$ = 560 V	4 – 5	—	—	50	µA	
On Resistance	$R_{DS(ON)}$	I_D = 41 mA	4 – 5	—	11.0	13.6	Ω	
Switching Time	t_f		4 – 5	—	—	250	ns	
Thermal Characteristics								
Thermal Resistance Junction to Case(1)(2)	θ_{J-C}		—	—	—	15	°C/W	STR5A464D
				—	—	16		STR5A464S

(1) Design assurance

(2) Case temperature (T_C) measured at the center of the case top surface

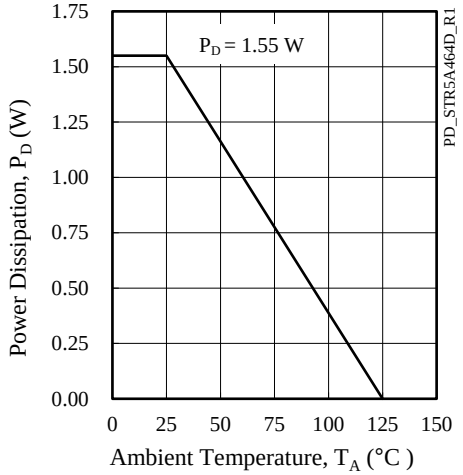
3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Package Weight		—	0.51	—	g	STR5A464D
		—	0.078	—	g	STR5A464S

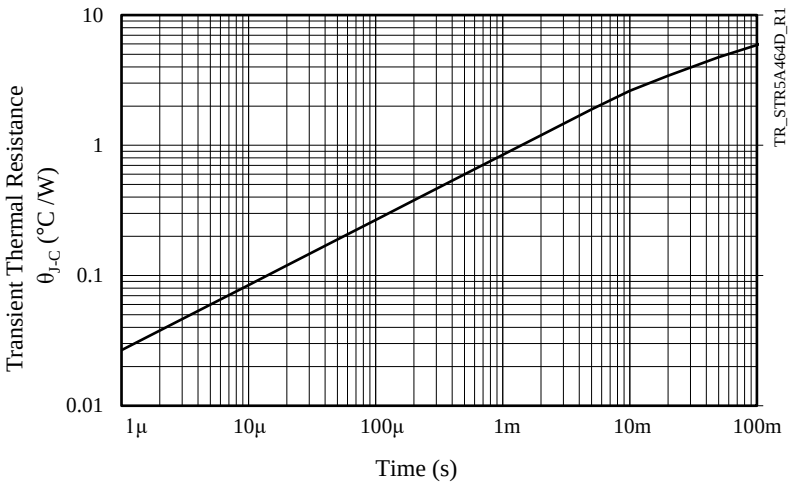
4. Performance Curves

● **STR5A464D**

Ambient Temperature versus Power Dissipation Curve

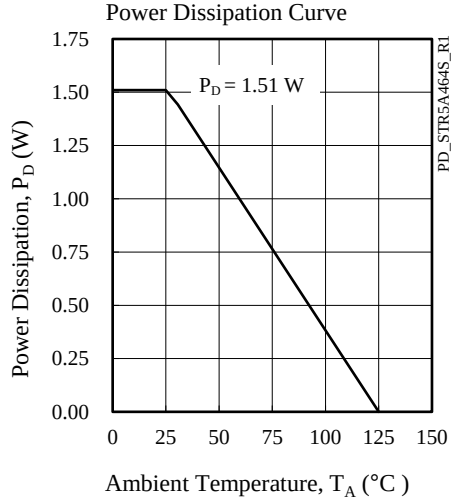


Transient Thermal Resistance Curve

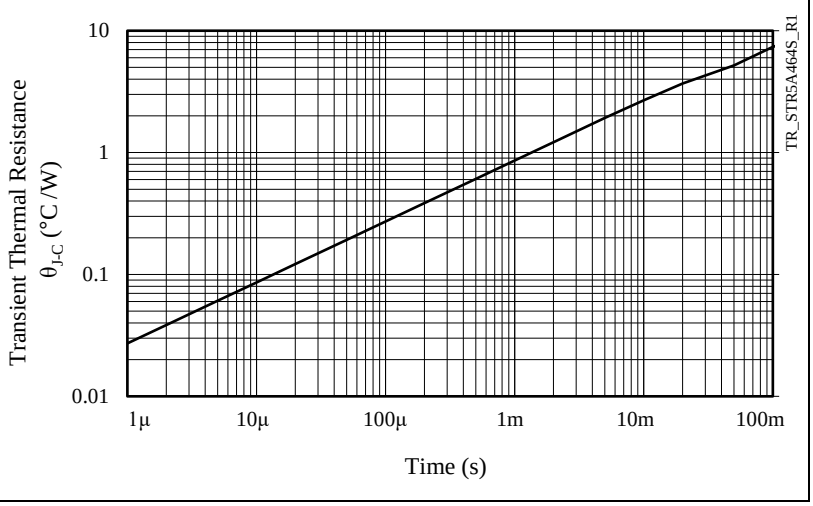


● **STR5A464S**

Ambient Temperature versus Power Dissipation Curve

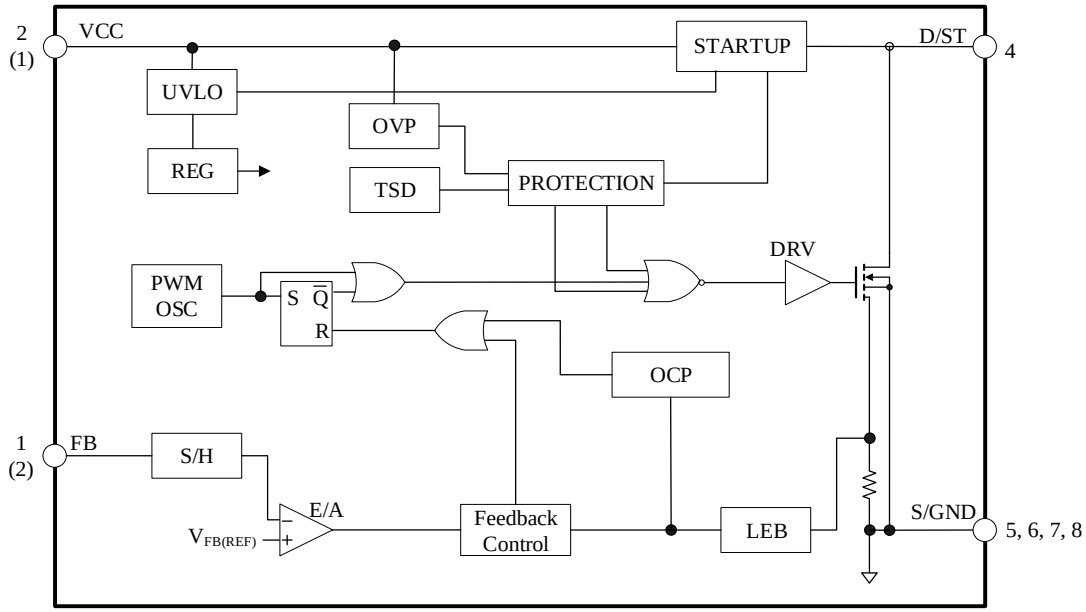


Transient Thermal Resistance Curve



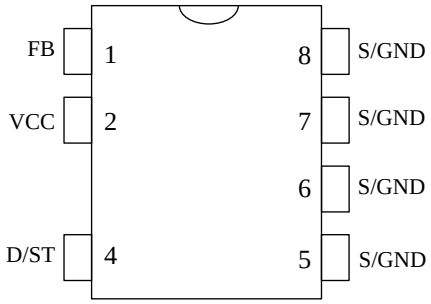
5. Block Diagram

The pin number of SOIC8 package products is shown in bracket.



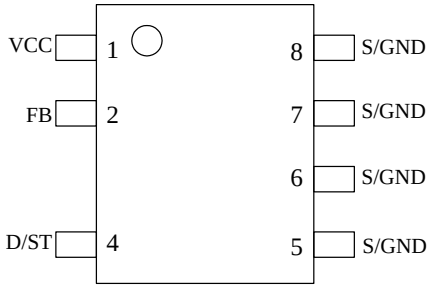
6. Pin Configuration Definitions

● DIP8



Pin	Name	Descriptions
1	FB	Constant voltage control signal input
2	VCC	Power supply voltage input for control part and overvoltage protection (OVP) signal input
3	—	(Pin removed)
4	D/ST	MOSFET drain and startup current input
5 to 8	S/GND	MOSFET source and ground

● SOIC8



Pin	Name	Descriptions
1	VCC	Power supply voltage input for control part and overvoltage protection (OVP) signal input
2	FB	Constant voltage control signal input
3	—	(Pin removed)
4	D/ST	MOSFET drain and startup current input
5 to 8	S/GND	MOSFET source and ground

7. Typical Application

Figure 7-1 and Figure 7-2 are the SOIC8 circuit example circuits of the buck and inverting converters.
To enhance the heat dissipation, the wide pattern layout of the S/GND pin (5 through 8 pin) is recommended.
When the absolute value of the output voltage | V_{OUT} | is 27.5 V or more, add a Zenner diode DZ1 connected to D1 in serial as shown in Figure 7-3. Using the maximum on-duty of 50 % in the steady state operation, the condition of $|V_{OUT}|$ is shown below:

| V_{OUT} | : $11V < |V_{OUT}| - V_{DZ1} < 27.5V$

| V_{OUT} | according to the input voltage:
For buck topology, | V_{OUT} | ≤ 0.5 × input voltage
For inverting topology, | V_{OUT} | ≤ input voltage

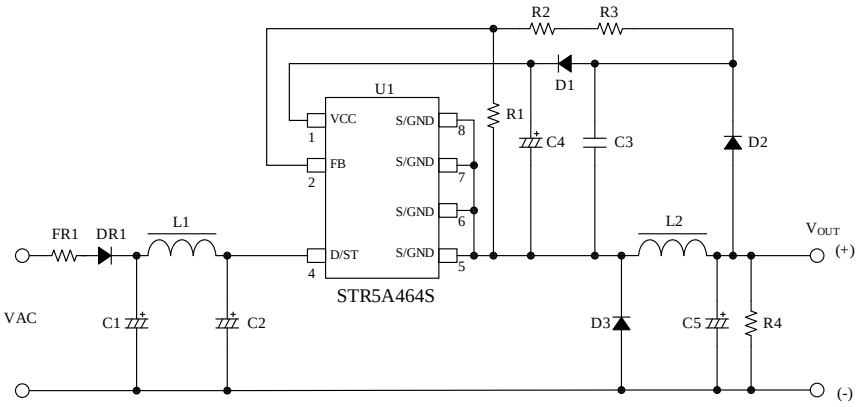


Figure 7-1. Buck Converter

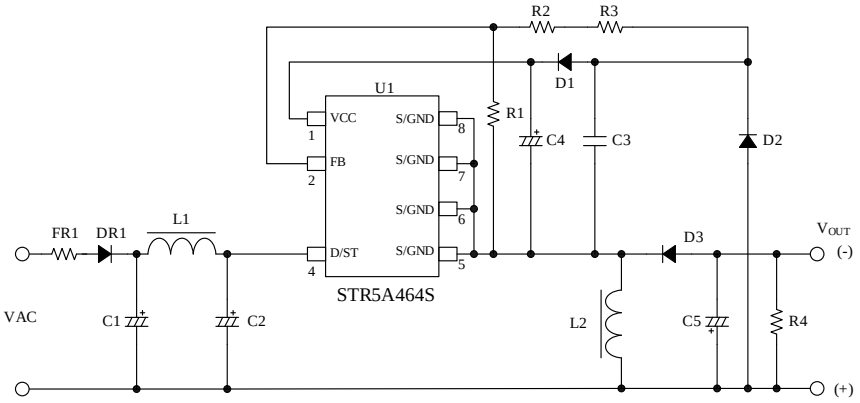


Figure 7-2. Inverting Converter

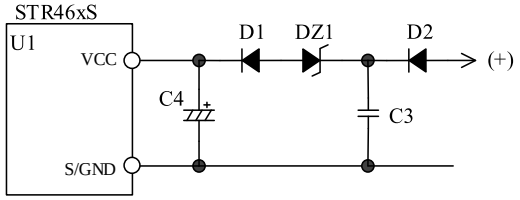
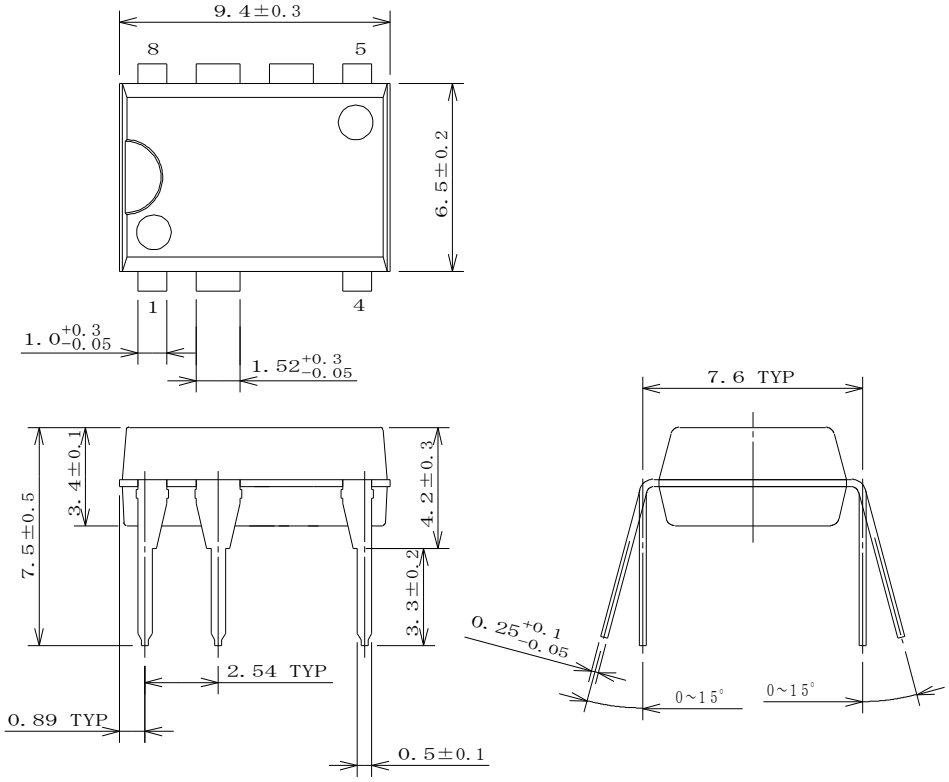


Figure 7-3. Increasing the Absolute Value of $|V_{OUT}|$

8. Physical Dimensions

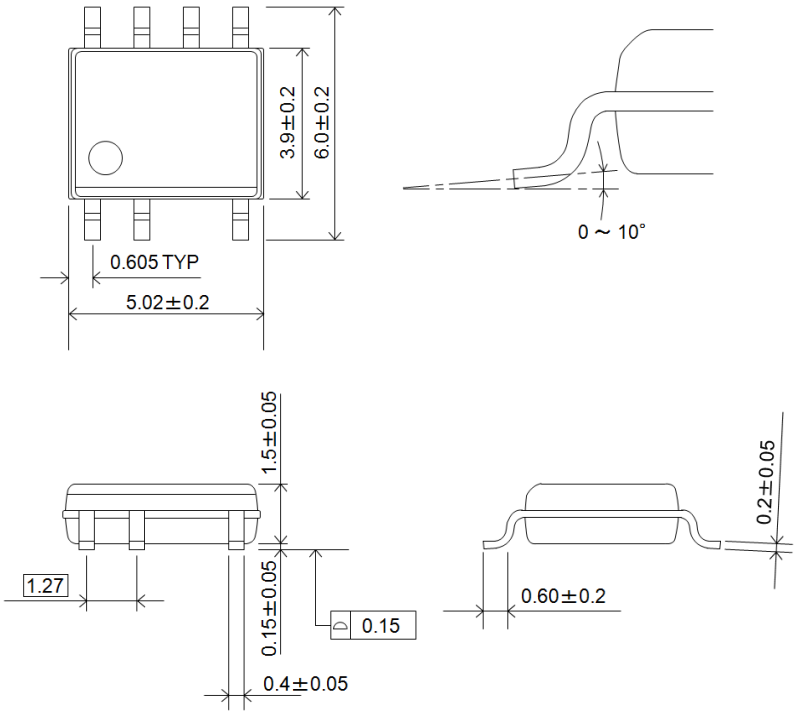
● **DIP8**



NOTES:

- All dimensions in millimeters
- Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 ℃ / 10 s, 1 time
  Soldering Iron: 350 ℃ / 3.5 s, 1 time
  Soldering should be at a distance of at least 1.5 mm from the body of the product.

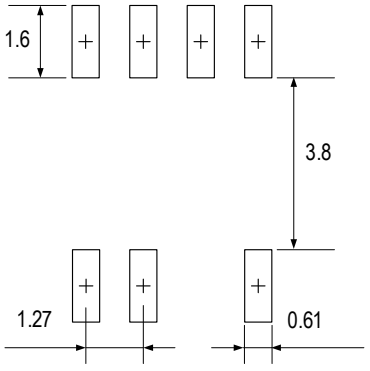
● **SOIC8**



NOTES:

- All dimensions in millimeters
- Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Soldering Iron: 350 °C / 3.5 s, 1 time

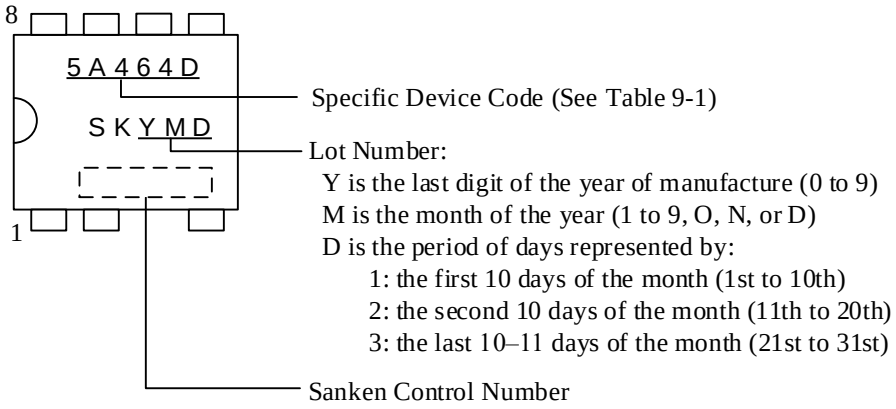
● **SOIC8 Land Pattern Example**



Unit: mm

9. Marking Diagram

● **DIP8**



● **SOIC8**

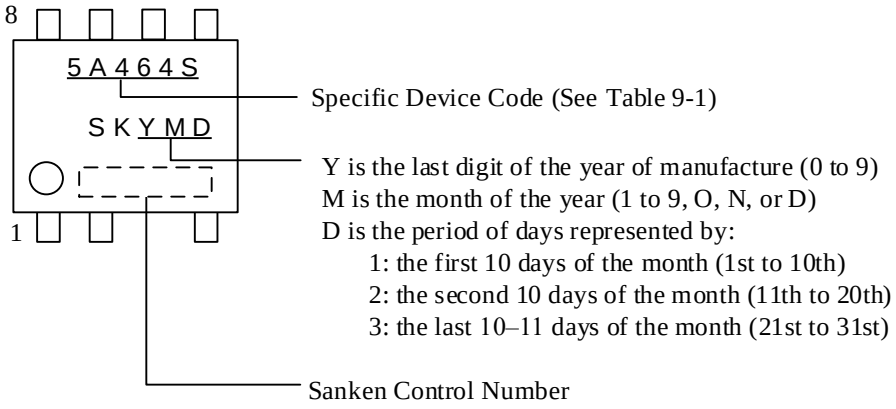


Table 9-1. Specific Device Code

Specific Device Code	Part Number
5A464D	STR5A464D
5A464S	STR5A464S

10. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

In Section 8, the pin number of SOIC8 package products is shown in bracket.

The common items of Buck converter and Inverting are desribed by using Buck conveter.

10.1 Startup Operation of IC

Figure 10-1 shows the circuit around VCC pin.

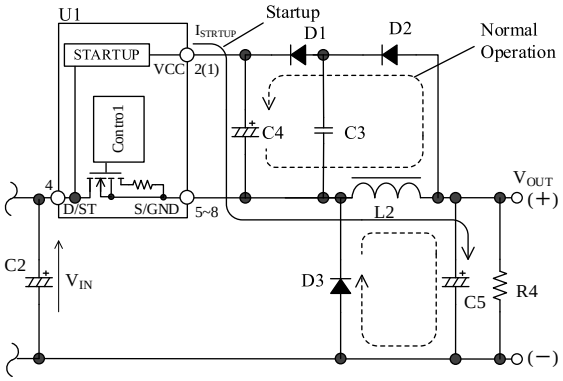


Figure 10-1. VCC Pin Peripheral Circuit in Buck Converter

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches the Startup Circuit Operation Voltage $V_{ST(ON)}$ = 29 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{CC(ST)}$ = −1.5 mA, charges C4 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts switching operation.

After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

The approximate startup time t_{START} is calculated as follows:

$$t_{START} = C4 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left|I_{CC(ST)}\right|} \ (s) \qquad (1)$$

where,

t_{START} is the startup time of IC (s),

$V_{CC(INT)}$ is the initial voltage on VCC pin (V).

When the internal power MOSFET turns off, the output voltage, V_{OUT}, charges C4 through D1 and D2 (see to Figure 10-1).

The voltage between VCC pin and S/GND pin in the steady state operation is calculated as follows, where V_{FD1}, V_{FD2} and V_{FD3} are the forward voltage of D1, D2 and D3 respectively:

$$V_{CC} = V_{OUT} + V_{FD3} - (V_{FD1} + V_{FD2}) \qquad (2)$$

10.2 Undervoltage Lockout (UVLO)

Figure 10-2 shows the relationship of VCC pin voltage and the circuit current, I_{CC}. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts switching operation and the circuit current, I_{CC}, increases. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.0 V, the control circuit stops its operation by the Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

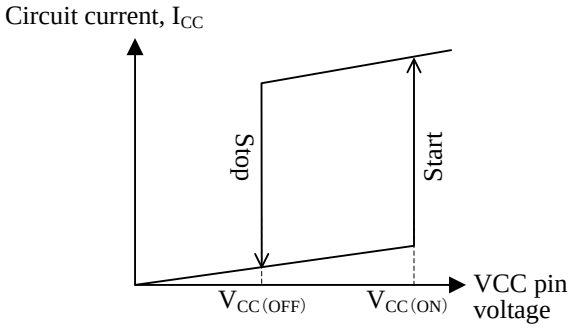


Figure 10-2. Relationship between VCC Pin Voltage and I_{CC}

10.3 Power Supply Startup and Soft Start Function

The soft start function reduces the voltage and the current stress of the internal power MOSFET and the freewheeling diode, D3.

Figure 10-3 shows the startup waveforms. After the IC starts, during the Standby Blanking Time at Startup, $t_{STB(INH)}$, the burst oscillation mode is disabled to operate the soft start.

The IC activates the soft start circuitry during the startup period. The soft start time is fixed to about 5.2 ms. During the soft start period, the overcurrent threshold is increased step-wisely (7 steps). The IC operates switching operation by the frequency responding to FB pin voltage until the output reaches the setting voltage.

Here, the t_{LIM} is defined as the period until FB pin voltage reaches 1.6 V after the IC starts. When the t_{LIM} reaches the OLP Delay Time at Startup, t_{OLP}, of 72 ms and more, the IC stops switching operation. Thus, it is

necessary to adjust the value of output electrolytic capacitor, C5 so that the t_{LIM} is less than t_{OLP}.

If VCC pin voltage reaches $V_{CC(OFF)}$ and a startup failure occurs as shown in Figure 10-4, increase C4 value or decrease C5 value. Since the larger capacitance causes the longer startup time of IC, it is necessary to check and adjust the startup process based on actual operation in the application.

Since the leading edge blanking function (see Section 10.5) is disabled during the soft start period, the on-time may be less than the Leading Edge Blanking Time (t_{BW} = 230 ns).

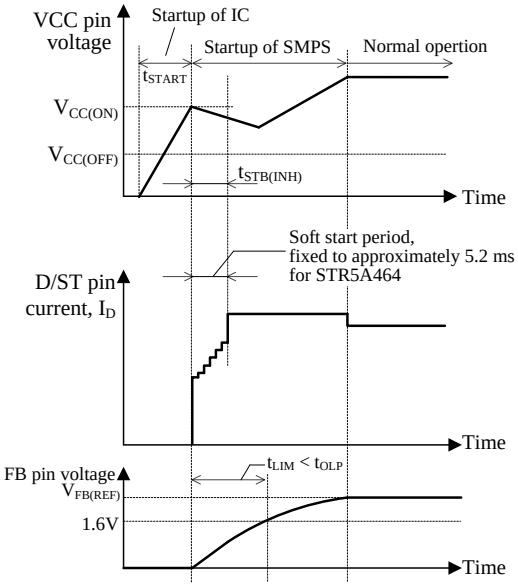


Figure 10-3. Startup Waveforms

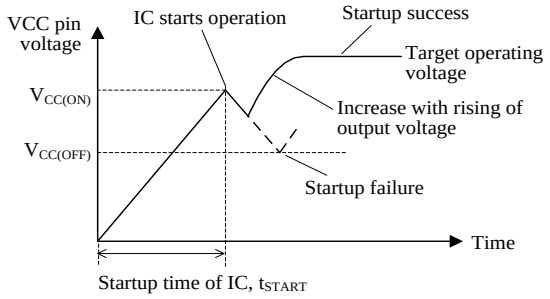


Figure 10-4. VCC Pin Voltage during Startup Period

10.4 Constant Voltage (CV) Control

The constant voltage (CV) control for power supply output adopts the peak-current-mode control method which enhances the response speed and the stable operation.

The target voltage, V_{SC}, is made from the voltage value sampled FB pin voltage on pulse by pulse basis at the point of t_{FBFS} = 2.5 µs (max.) after turning off the internal power MOSFET. The V_{ROCP} is the voltage value of the built-in drain current sense resistor. The IC controls so that the peak voltage of V_{ROCP} is close to V_{SC} by comparing them at the internal FB comparator (see Figure 10-5 and Figure 10-6).

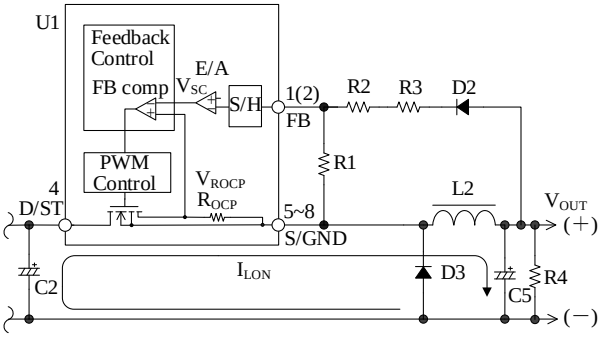


Figure 10-5. FB Pin Peripheral Circuit in Buck Converter

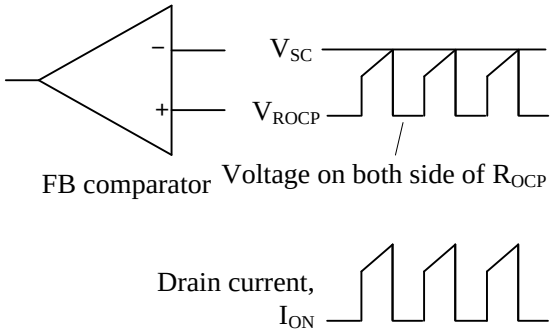


Figure 10-6. Drain Current I_D and FB Comparator in Steady State Operation

- Decreasing Load
  When the output load decreases, the FB pin voltage increases in response to the increase of the output voltage. Since V_{SC} which is the output voltage of internal error amplifier becomes low, the peak value of V_{ROCP} is controlled to become low, and the peak of the drain current decreases. This control prevents the output voltage from increasing.

- Increasing Load
  When the output load increases, the control circuit operates the reverse of the former operations. Since V_{SC} becomes high, the peak drain current increases. This control prevents the output voltage from decreasing.

10.4.1 Buck Converter Operation

Figure 10-7 shows the output current path in the Buck converter. Figure 10-8 shows the operational waveforms.

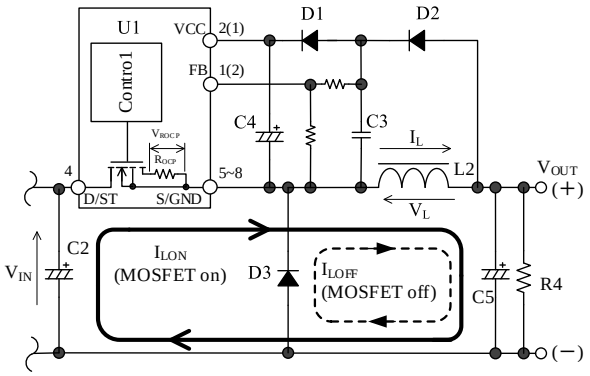


Figure 10-7. Output Current Path in Buck Converter

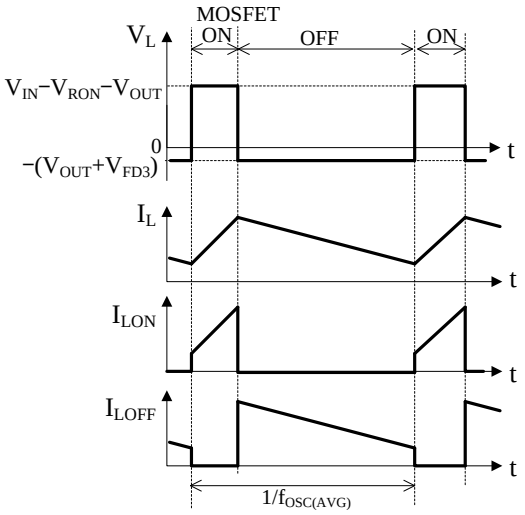


Figure 10-8. Operational Waveforms in Buck Converter

In the Buck converter, the PWM control is described in the following.

1) PWM On-Time Period
When the internal power MOSFET turns on, the I_{LON} current flows as shown in Figure 10-7, and the inductor, L2, stores some energy.
Since the I_{LON} flows through the internal sense resistor, R_{OCP}, the voltage of R_{OCP} is detected as the current detection voltage, V_{ROCP}.
FB pin voltage is the voltage divided C3 voltage by voltage dividing resistors, and the target voltage, V_{SC}, is given by FB pin voltage.
When V_{ROCP} reaches V_{SC}, the power MOSFET turns off.

2) PWM Off-Time Period
When the internal power MOSFET turns off, the back electromotive force occurs in the inductor, L2, the freewheeling diode, D3, is forward biased and turns on. Thus, the I_{LOFF} current flows as shown in Figure 10-7.
As shown in Figure 10-8, after the average switching period, $1/f_{OSC(AVG)}$, the power MOSFET turns on again, and the event moves to the previous 1).

The output current is equal to the average inductor current of L2.

10.4.2 Inverting Converter Operation

Figure 10-9 shows the output current path in the Inverting converter. Figure 10-10 shows the operational waveforms.

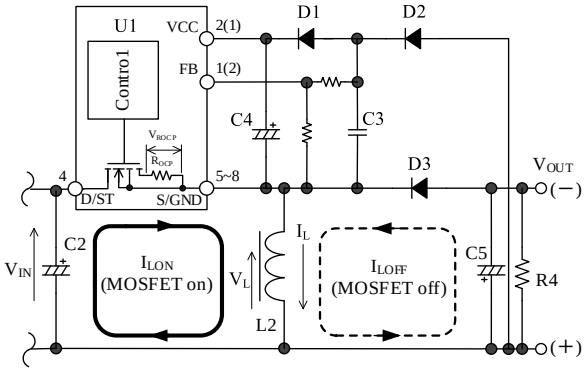


Figure 10-9. Output Current Path in Inverting Converter

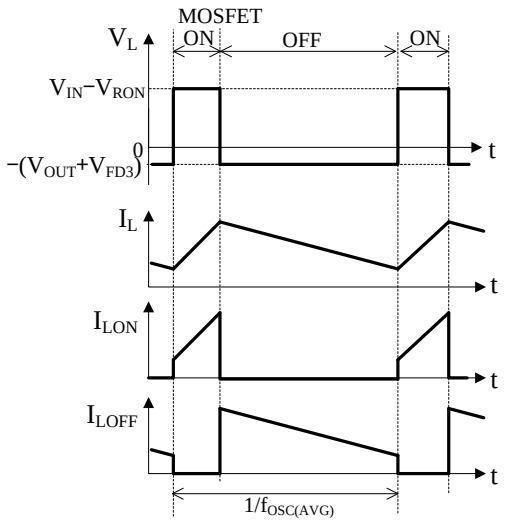


Figure 10-10. Operational Waveforms in Inverting Converter

In the Inverting converter, the PWM control is described in the following.

1) PWM On-Time Period
When the internal power MOSFET turns on, the I_{LON} current flows as shown in Figure 10-9, and the inductor, L2, stores some energy. Since the I_{LON} flows through the internal sense resistor, R_{OCP}, the voltage of R_{OCP} is detected as the current detection voltage, V_{ROCP}. FB pin voltage is the voltage divided C3 voltage by voltage dividing resistors, and the target voltage, V_{SC}, is given by FB pin voltage. When V_{ROCP} reaches V_{SC}, the power MOSFET turns off.

2) PWM Off-Time Period
When the internal power MOSFET turns off, the back electromotive force occurs in the inductor, L2, the freewheeling diode, D3, is forward biased and turns on. Thus, the I_{LOFF} current flows as shown in Figure 10-9. As shown in Figure 10-10, after the average switching period, $1/f_{OSC(AVG)}$, the power MOSFET turns on again, and the event moves to the previous 1).

The output current is equal to the average current of I_{LOFF} of L2.

10.5 Leading Edge Blanking Function

The constant voltage control for power supply output adopts the peak-current-mode control method. The peak drain current is detected by the internal sense resistor, R_{OCP}. Just in turning on the internal power MOSFET, the steep surge current would occur.

If the overcurrent protection (OCP) responds to the voltage caused by that surge current, the power MOSFET may be turned off.

To prevent that response, the OCP detection is disabled during Leading Edge Blanking (t_{BW} = 230 ns) just after the power MOSFET turns on.

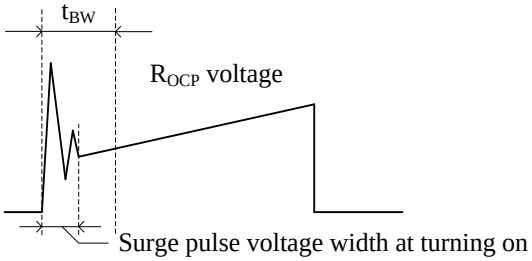


Figure 10-11. Leading Edge Blanking

10.6 Random Switching Function

The switching frequency is randomly modulated by superposing the modulating frequency on $f_{OSC(AVG)}$. This function reduces the conduction noise compared with other products without this function, and simplifies noise filtering of the input lines of power supply.

10.7 Operation Mode

As shown in Figure 10-12, when the output power is decreasing, together with the decrease of the drain current I_D of the internal power MOSFET, the operation mode is automatically changed to the fixed switching frequency mode (60 kHz), to the green mode controlled the switching frequency (23 kHz to 60 kHz), and to the burst oscillation mode controlled by an internal oscillator. In the green mode, the number of switching is reduced. In the burst oscillation mode, the switching operation is stopped during a constant period. Thus, the switching loss is reduced, and the power efficiency is improved.

When the output power becomes light and the drain current decreases to the Standby Drain Current, I_{DSTB}, the burst oscillation mode is getting started. Figure 10-13 shows the drain current waveforms of point A and B in Figure 10-12. The burst period of burst oscillation mode is the Standby Operation Cycle, t_{STBOP} = 740 µs. In the burst period, the number of minimum switching times is reduced up to one.

Since the oscillator for setting burst oscillation cycle and the oscillator for setting the switching oscillation frequency are not synchronized each other, the first switching frequency in the burst period may be raised.

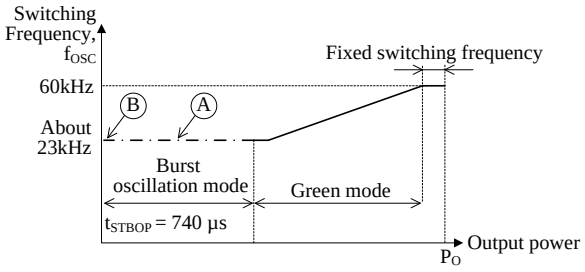


Figure 10-12. Switching Frequency in Response to Output Power

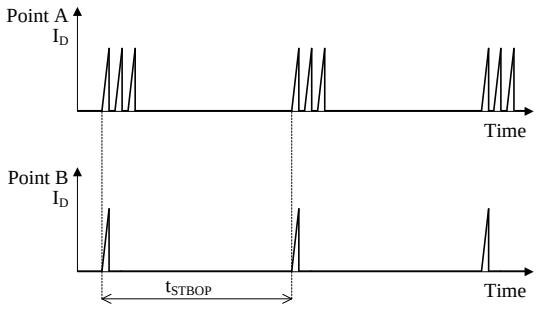


Figure 10-13. Switching Waveform at Burst Oscillation Mode

10.8 Overload Protection (OLP)

When the drain current, I_D, reaches the Drain Current Limit, I_{DLIM}, the internal power MOSFET turns off. Figure 10-14 shows the characteristic of output voltage and current.

The output voltage decreases in the overload state, and FB pin voltage also decreases. When the period keeping FB pin voltage less than 1.6 V continues during the OLP Delay Time at Startup (t_{OLP} = 72 ms), the overload protection (OLP) is activated, and the IC stops switching operation. Thus, VCC pin voltage decreases to $V_{CC(OFF)}$, and the control circuit stops operation. After that, the startup circuit is activated, VCC pin voltage increases to $V_{CC(ON)}$ by the startup current, and the control circuit operates again. Thus, the intermittent operation by UVLO is repeated in the OLP state (see Figure 10-15). This intermittent operation reduces the stress of parts including the power MOSFET and the freewheeling diode. In addition, this operation reduces power consumption because the switching period in this intermittent operation is much shorter than the oscillation stop period. When the abnormal condition is removed, the IC returns to normal operation automatically.

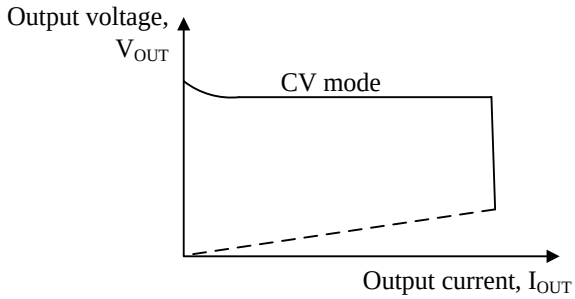


Figure 10-14. Overload Characteristics

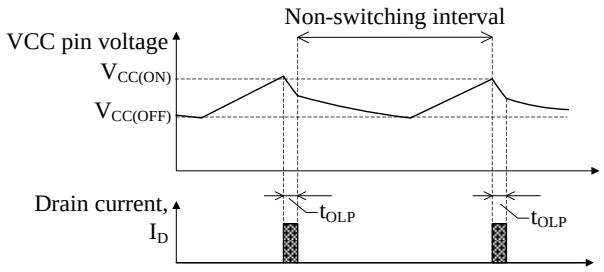


Figure 10-15. OLP Operational Waveform

10.9 Overvoltage Protection (OVP)

When the voltage between VCC pin and S/GND pin increases to $V_{CC(OVP)}$ = 29.3 V or more, the overvoltage protection (OVP) is activated and the IC stops switching operation. The intermittent operation by UVLO is repeated in the OVP state. See Section 10.8 about the intermittent operation by UVLO.

When the abnormal condition is removed, the IC returns to normal operation automatically.

The approximate value of output voltage $V_{OUT(OVP)}$ in the OVP condition is calculated by using Equation (3).

$$V_{OUT(OVP)} = V_{CC(OVP)} + V_{FD1} + V_{FD2} - V_{FD3} \quad (3)$$

where,
$V_{OUT(OVP)}$ is voltage of between $V_{OUT}(+)$ and $V_{OUT}(-)$,
V_{FD1} is the forward voltage of D1 in Figure 10-1,
V_{FD2} is the forward voltage of D2, and
V_{FD3} is the forward voltage of D3.

10.10 Thermal Shutdown (TSD)

Figure 10-16 shows the thermal shutdown (TSD) operational waveforms.

When the junction temperature of the IC control circuit increases to $T_{J(TSD)}$ = 135 °C (min.) or more, the TSD is activated, and the IC stops switching operation. The TSD has a temperature hysteresis. When VCC pin voltage decreases to about 9.4 V during the $T_J > (T_{J(TSD)}-T_{J(TSD)HYS})$, the startup circuit supplies startup current to VCC pin to keep the VCC pin voltage > $V_{CC(OFF)}$.

While the junction temperature is $T_{J(TSD)}-T_{J(TSD)HYS}$ or less, the startup circuit stops the startup current supply. Then, VCC pin voltage decreases to $V_{CC(OFF)}$ or less, and the control circuit stops operation. After that, the startup circuit is activated, VCC pin voltage increases to $V_{CC(ON)}$ by the startup current, and the control circuit operates again. The intermittent operation by TSD and UVLO is repeated in the TSD state.

After the fault condition is removed, the IC returns to normal operation automatically.

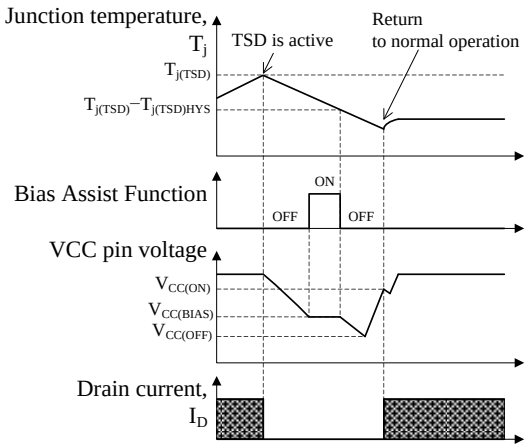


Figure 10-16. TSD Operational Waveforms

11. Design Notes

11.1 External Components

Take care to use properly rated, including derating as necessary, and proper type of components.

Figure 11-1 shows the peripheral circuit of IC in Buck converter. The pin number of SOIC8 package products in the circuits is shown in bracket.

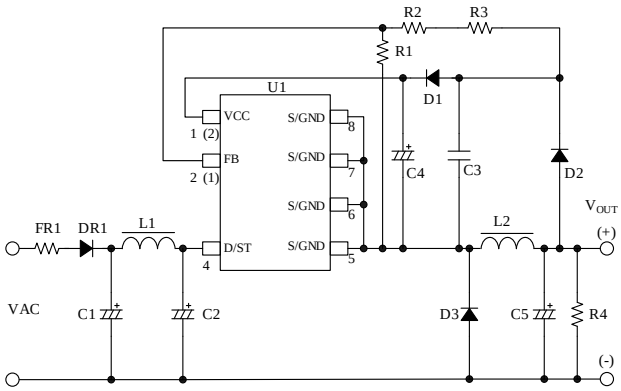


Figure 11-1. Peripheral Circuit of IC in Buck Converter

11.1.1 Input and Output Electrolytic Capacitor

Apply proper derating to ripple current, voltage, and temperature rise.

The value of output electrolytic capacitor, C5, should be fulfilled the following conditions:

- The specification of output ripple
- Enough shorter output voltage rising time in startup than the OLP Delay Time at Startup, t_{OLP} = 72 ms.
- Low impedance types, designed for switch mode power supplies, is recommended.

The ESR of C5 should be set in the range of Equation (4).

$$Z_{CO} < \frac{\Delta V_{OR}}{I_{LRP}} \quad (4)$$

where,

Z_{CO} is the ESR of electrolytic capacitor at the operation frequency (Since the ESR in general catalogs is mostly measured at 100 kHz, check the frequency characteristic.),

ΔV_{OR} is the output ripple voltage specification, and

I_{LRP} is the ripple current of inductor.

11.1.2 Inductor

Apply proper design margin to core temperature rise by core loss and copper loss.

The inductor should be designed so that the inductor current does not saturate. The inductance should be the minimum considered a negative tolerance of inductance and a decline of DC superposition characteristics.

The on-time must be longer than the Leading Edge Blanking Time to control the output voltage constantly.

In the universal input voltage design, the on-time is easy to become short in the condition of maximum AC input voltage and light load. Be careful not to choose too small value for the inductance (The recommended value is 600 µH or more).

Refer to the following design example of how to the inductor setting of the buck converter.

- DEE0012 Design Example Using STR5A464S: 3 W (15 V, 0.2 A) Offline Buck Converter
  https://www.semicon.sanken-ele.co.jp/common/pdf/designexample/dee0012.pdf

11.1.3 VCC Pin Peripheral Circuit

The reference value of C4 in Figure 11-1 is generally 10 to 47 µF. See Section 10.1 about the startup time.

11.1.4 FB Pin Peripheral Circuit

As shown in Figure 11-1, FB pin is input the voltage divided the voltage between V_{OUT}(+) and S/GND pin by resistors.

C3 is the smoothing capacitor. The value of C3 depends on the value of output electrical capacitor, C5. Usually the value of C3 is 0.068 µF to 0.47 µF. When C3 value is set larger, the line regulation becomes better, however, the dynamic response of the output voltage becomes worse. Be careful of that value.

The voltage dividing resistor of R1, R2 and R3 is determined by the reference voltage, $V_{FB(REF)}$ = 2.50 V, the output voltage, V_{OUT}, and so on. The following Equation (5) shows the relationship of them.

The target value of R1 is about 5.6 kΩ to 10 kΩ. R2 and R3 should be adjusted in actual operation condition.

The V_F of D2 and D3 affects the output voltage. Thus, the diodes of low V_F should be selected.

$$|V_{OUT}| \cong V_{FB(REF)} \times \frac{R1 + R2 + R3}{R1} + V_{FD2} - V_{FD3}$$

$$\Rightarrow R2 + R3 = \left(\frac{|V_{OUT}| - V_{FD2} + V_{FD3}}{V_{FB(REF)}} - 1 \right) \times R1 \quad (5)$$

where,
V_{FD2} is the forward voltage of D2, and
V_{FD3} is the forward voltage of D3.

11.1.5 Freewheeling Diode

D3 in Figure 11-1 is the freewheeling diode.

When the internal power MOSFET turns on, the recovery current flows through D3. The current affects power loss and noise much. The V_F affects the output voltage. Thus, the diode of fast recovery and low V_F should be selected.

11.1.6 Bleeder Resistance

For light load application, the bleeder resistor, R4, in Figure 11-1 should be connected to both ends of output capacitor, C5, to prevent the increase of output voltage.

The value of R4 should be satisfied with Equation (6), and should be adjusted in actual operation condition.

$$R4 \leq \frac{|V_{OUT}|}{3mA} \quad (6)$$

11.2 D/ST Pin

When the D/ST pin voltage and the current exceed the Absolute Maximum Ratings, the internal power MOSFET connected to D/ST pin would be permanently damaged. The D/ST pin voltage should be less than 630 V which is the derating value of 90% for the Absolute Maximum Ratings, 700 V, in all condition of actual operation, and the parameters of transformer and components value should be selected based on actual operation in the application.

In addition, the D/ST pin voltage should be less than 560 V in the steady state operation.

11.3 PCB Trace Layout

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace. In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account. Figure 11-2 and Figure 11-3 show the circuit design example.

1) Main Circuit Trace Layout
   This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

2) Freewheeling Loop Layout
   This is the trace for the current of freewheeling diode, D3, and thus it should be as wide trace and small loop as possible.

3) Control Ground Trace Layout
   Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at single point grounding.

4) VCC Trace Layout
   This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C4 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the S/GND pin is recommended.

5) FB Trace Layout
   The divided voltage by R2+R3 and R1 of output voltage is input to the FB pin.
   To increase the detection accuracy, R3 and R1 should be connected to the bottom of C3 and the S/GND pin, respectively. The trace between R1, R2 and the FB pin should be as short as possible.

6) Thermal Considerations
   Since the internal power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.
   Since the copper area under the IC and the S/GND pin trace act as a heatsink, its traces should be as wide as possible.

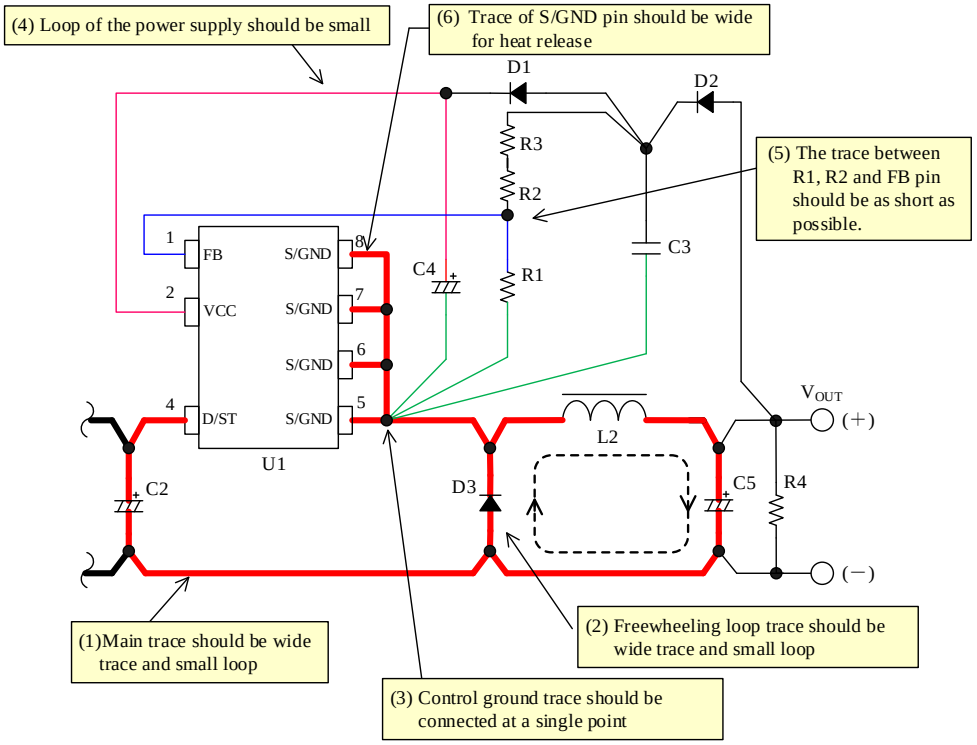


Figure 11-2. Peripheral Circuit Example Around IC for Buck Converter (DIP8)

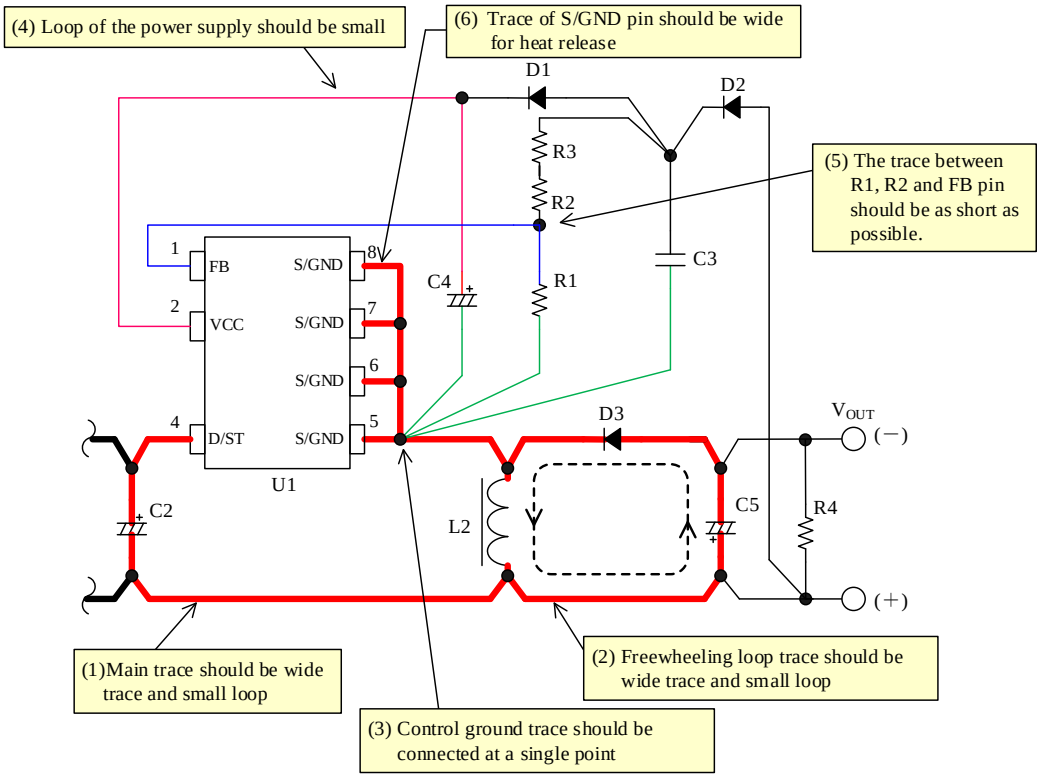
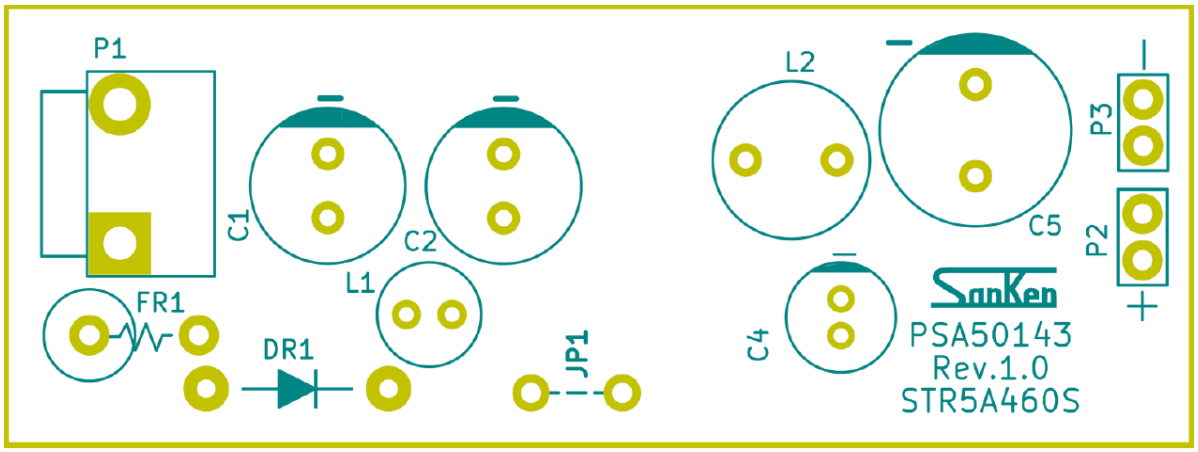


Figure 11-3. Peripheral Circuit Example Around IC for Inverting Converter (DIP8)

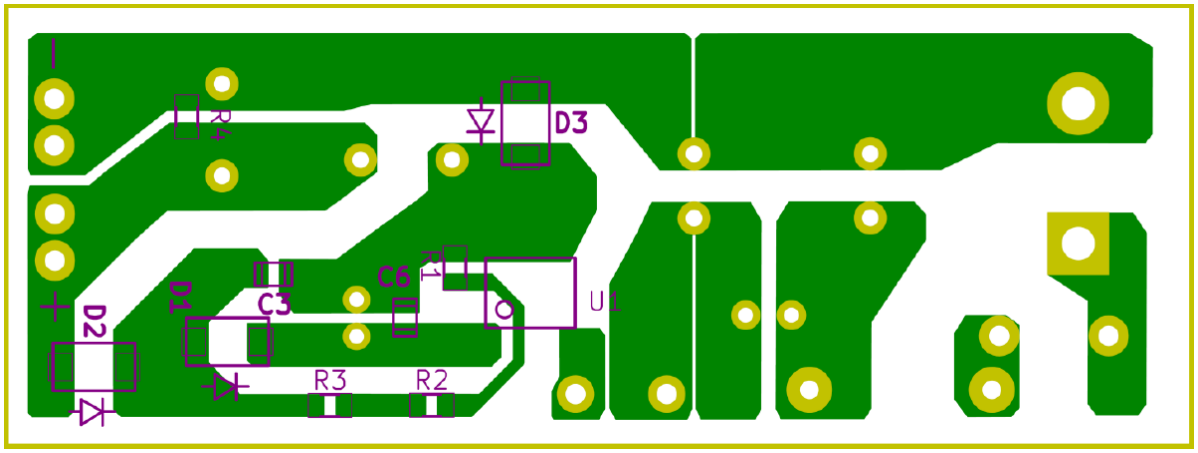
12. Pattern Layout Example (Buck Converter)

The following show the pattern layout example and the circuit schematic for the buck converter using STR5A464S. The design example uses only the parts listed in the circuit diagram and the bill of materials.

PCB dimensions: 65 mm × 24 mm



(a) Top View



(b) Bottom View

Figure 12-1. Pattern Layout Example for Buck Converter

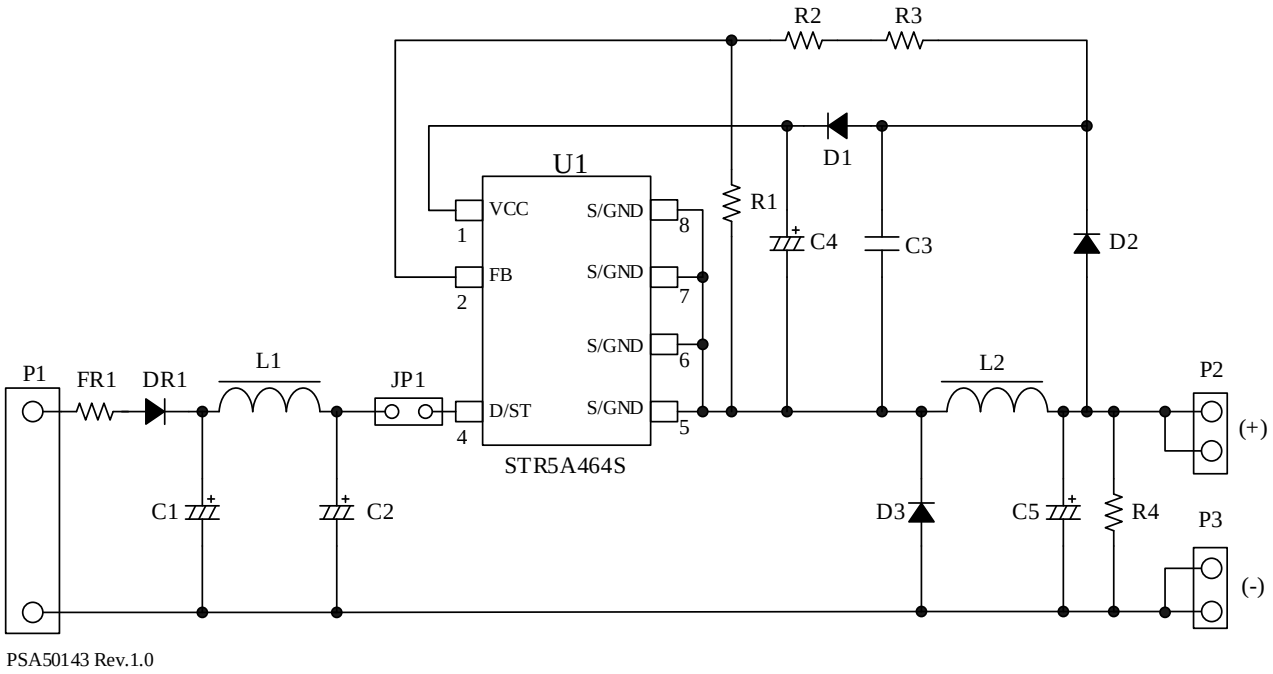


Figure 12-2. Circuit Diagram for Buck Converter

13. Design Example

The following show the power supply specification, the circuit schematic, and the bill of materials of the buck converter reference design.

- Power Supply Specification

IC	STR5A464S
Input voltage	85 VAC to 265 VAC
Maximum output power	3 W
Output voltage	15 V
Output current	0.2 A

- Circuit Diagram

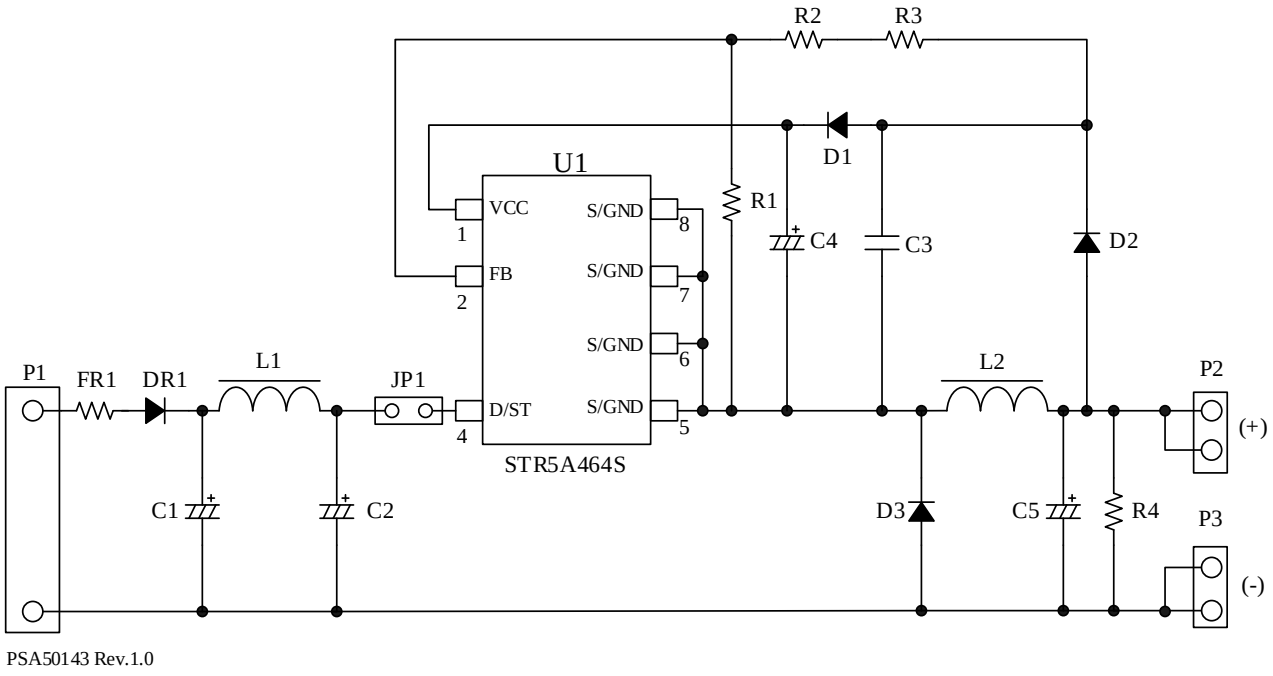


Figure 13-1. Circuit Diagram for Buck Converter

● Bill of Materials

Symbol	Part Type	Ratings	Recommended Sanken Parts
C1	Electrolytic capacitor	105 °C, 400 V, 8.2 µF	
C2	Electrolytic capacitor	105 °C, 400 V, 8.2 µF	
C3	Ceramic capacitor	50 V, 0.22 µF, 2012	
C4	Electrolytic capacitor	105 °C, 50 V, 10 µF	
C5	Electrolytic capacitor	105 °C, 25 V, 470 µF	
DR1	General-purpose rectifier diode	1000 V, 1 A	EM1C
D1	Schottky diode	90 V, 1 A	SJPB-D9
D2	Fast recovery diode	500 V, 1 A	SJPD-D5
D3	Fast recovery diode	500 V, 1 A	SJPD-D5
L1	Inductor	1 mH, 0.21 A	
L2	Inductor	1 mH, 0.5 A	
FR1	Resistor	2 W, 10 Ω	
R1	Chip resistor	6.8 kΩ, 1/8 W, 1608	
R2	Chip resistor	33 kΩ, 1/8 W, 1608	
R3	Chip resistor	1.8 kΩ, 1/8 W, 1608	
R4	Chip resistor	6.8 kΩ, 1/8 W, 1608	
U1	PWM offline converter IC	700 V, 13.6 Ω	STR5A464S
JP1	Jumper wire	Plated wire (φ = 0.6, P = 5 mm)	
P1	Connector	250 V	
P2	Connector	50 V	
P3	Connector	50 V	
—	PCB	PSA50143 Rev.1.0	

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