Off-line PWM Controllers with Integrated Power MOSFET

STR6A124MV

Data Sheet

Description

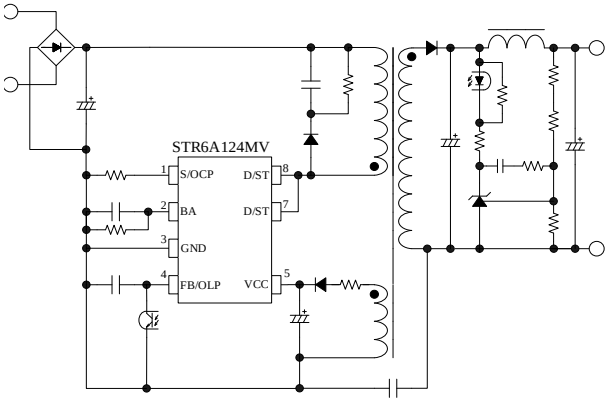
The STR6A124MV is power IC for switching power supplies, incorporating a MOSFET and a current mode PWM controller IC.

To enhance efficiency in all load ranges, the IC automatically shifts its operation to the green mode or burst oscillation mode, depending on the load. The product achieves high cost-performance power supply systems with few external components.

Features

- Improving Circuit Efficiency
  (Since the step drive control can keep V_{RM} of secondary rectification diodes low, the circuit efficiency can be improved by low V_F)
- Current Mode Type PWM Control
- Soft Start Function
- Adjustable Standby Operating Point
  No Load Power Consumption < 15 mW
- Operation Mode
  Fixed Frequency: 65 kHz
  Green-mode: 25 kHz to 65 kHz
  Burst Oscillation Mode
- Random Switching Function
- Slope Compensation Function
- Leading Edge Blanking Function
- Bias Assist Function
- Protections
  Two Types of Overcurrent Protection (OCP): Pulse-by-Pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
  Overload Protection with Timer (OLP): Auto-restart
  Overvoltage Protection (OVP): Latched shutdown
  Thermal Shutdown (TSD): Latched shutdown

Typical Application



Package

DIP8

Not to Scale

Specifications

- $f_{OSC(AVG)}$ (typ.) = 65 kHz
- V_{DSS} (min.) = 700 V
- $R_{DS(ON)}$ (max.) = 1.4 Ω
- Output Power, P_{OUT} (1)

Part Number	Adapter		Open Frame	
	AC230V	AC85 ~265V	AC230V	AC85 ~265V
STR6A124MV	29 W	23 W	46 W	33 W

Applications

- White Goods
- Office Automation Equipment
- Audio Visual Equipment
- Industrial Equipment
- Other Switched-mode Power Supply

(1) The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, duty cycle, and thermal design affect the output power. It may be less than the value stated here.

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C, 7 pin = 8 pin.

Parameter	Symbol	Conditions	Pins	Rating	Unit	Remarks
Drain Peak Current [1]	I_{DPEAK}	Single pulse	8 − 1	4.0	A	
Maximum Drain Current	I_{DMAX}	T_A = − 40 to 125 °C	8 − 1	4.0	A	
Avalanche Energy[2][3]	E_{AS}	I_{LPEAK} = 0.5 A	8 – 1	2.9	mJ	
S/OCP Pin Voltage	$V_{S/OCP}$		1 − 3	−2 to 6	V	
BA Pin Voltage	V_{BA}		2 − 3	−0.3 to 7.5	V	
BA Pin Sink Current	I_{BA}		2 − 3	1.0	mA	
FB/OLP Pin Voltage	V_{FB}		4 − 3	−0.3 to 14	V	
FB/OLP Pin Sink Current	I_{FB}		4 − 3	1.0	mA	
VCC Pin Voltage	V_{CC}		5 − 3	−0.3 to 32	V	
D/ST Pin Voltage	$V_{D/ST}$		8 − 3	−1 to V_{DSS}	V	
MOSFET Power Dissipation[4]	P_{D1}	[5]	8 − 1	1.35	W	
Control Part Power Dissipation	P_{D2}		5 − 3	1.2	W	
Operating Ambient Temperature	T_{OP}		—	−40 to 125	°C	
Storage Temperature	T_{STG}		—	−40 to 125	°C	
Junction Temperature	T_J		—	150	°C	

[1] See Section 4.2.
[2] See Figure 4-2.
[3] Single pulse, V_{DD} = 99 V, L = 20 mH.
[4] See Section Figure 4-3.
[5] When embedding this hybrid IC onto the printed circuit board (copper area in a 15 mm × 15 mm).

2. Electrical Characteristics

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, T_A = 25 °C, V_{CC} = 18 V, 7 pin = 8 pin.

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit	Remarks
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		5 − 3	13.8	15.0	16.2	V	
Operation Stop Voltage*	$V_{CC(OFF)}$		5 − 3	7.6	8.5	9.2	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	5 − 3	—	1.5	3.0	mA	
Startup Circuit Operation Voltage	$V_{ST(ON)}$		8 − 3	40	47	55	V	
Startup Current	$I_{CC(ST)}$	V_{CC} = 13.5 V	5 − 3	−4.05	−2.50	−1.08	mA	
Startup Current Biasing Threshold Voltage*	$V_{CC(BIAS)}$	I_{CC} = −500 µA	5 − 3	8.0	9.6	10.5	V	
Normal Operation								
Average Switching Frequency	$f_{OSC(AVG)}$		8 − 3	58	65	72	kHz	
Switching Frequency Modulation Deviation	Δf		8 − 3	—	5.4	—	kHz	
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V	4 − 3	−170	−130	−85	µA	
Minimum Feedback Current	$I_{FB(MIN)}$		4 − 3	−21	−13	−5	µA	
Light Load Operation								
FB/OLP Pin Starting Voltage of Frequency Decreasing	$V_{FB(FDS)}$	$f_{OSC(AVG)}$ × 0.9	4 − 3	2.64	3.30	3.96	V	
FB/OLP Pin Ending Voltage of Frequency Decreasing	$V_{FB(FDE)}$	$f_{OSC(MIN)}$ × 1.1	4 − 3	2.40	3.00	3.60	V	
Minimum Switching Frequency	$f_{OSC(MIN)}$		8 − 3	18	25	32	kHz	
Standby Operation								
FB/OLP Pin Oscillation Stop Threshold Voltage 1	$V_{FB(OFF1)}$	R_{BA}: Short	4 − 3	1.17	1.28	1.39	V	
FB/OLP Pin Oscillation Stop Threshold Voltage 2	$V_{FB(OFF2)}$	R_{BA}: Open	4 − 3	1.50	1.63	1.76	V	
FB/OLP Pin Oscillation Stop Threshold Voltage 3	$V_{FB(OFF3)}$	R_{BA}: 330 kΩ	4 − 3	1.78	1.92	2.06	V	
FB/OLP Pin Oscillation Stop Threshold Voltage 4	$V_{FB(OFF4)}$	R_{BA}: 68 kΩ	4 − 3	2.02	2.17	2.32	V	
Protection								
Maximum Duty Cycle	D_{MAX}		8 − 3	70	75	80	%	
Leading Edge Blanking Time	t_{BW}		—	—	330	—	ns	
OCP Compensation Coefficient	DPC		—	—	17.3	—	mV/µs	

* $V_{CC(BIAS)} > V_{CC(OFF)}$ always.

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Unit	Remarks
OCP Compensation Duty Cycle	D_{DPC}		—	—	36	—	%	
OCP Threshold Voltage at Zero Duty Cycle	$V_{OCP(L)}$		1 − 3	0.735	0.795	0.855	V	
OCP Threshold Voltage at 36% Duty Cycle	$V_{OCP(H)}$		1 − 3	0.843	0.888	0.933	V	
OCP Threshold Voltage in Leading Edge Blanking Time	$V_{OCP(LEB)}$		1 − 3	—	1.69	—	V	
OLP Threshold Voltage	$V_{FB(OLP)}$		4 − 3	6.8	7.3	7.8	V	
OLP Delay Time	t_{OLP}		4 − 3	55	75	90	ms	
OLP Operation Current	$I_{CC(OLP)}$		5 − 3	—	260	—	µA	
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		4 − 3	10.5	11.8	13.5	V	
OVP Threshold Voltage	$V_{CC(OVP)}$		5 − 3	27.0	29.1	31.2	V	
Thermal Shutdown Operating Temperature	$T_{J(TSD)}$		—	127	145	—	°C	
MOSFET								
Drain-to-Source Breakdown Voltage	V_{DSS}	I_{DS} = 300 µA	8 − 1	700	—	—	V	
Drain Leakage Current	I_{DSS}	$V_{DS} = V_{DSS}$	8 − 1	—	—	300	µA	
On-resistance	$R_{DS(ON)}$	I_{DS} = 0.4 A	8 − 1	—	—	1.4	Ω	
Switching Time	t_f		8 − 1	—	—	250	ns	
Thermal Resistance								
Junction-to-Case	θ_{J-C}		—	—	—	22	°C/W	

3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.51	—	g

4. Performance Curves

4.1. Derating Curves

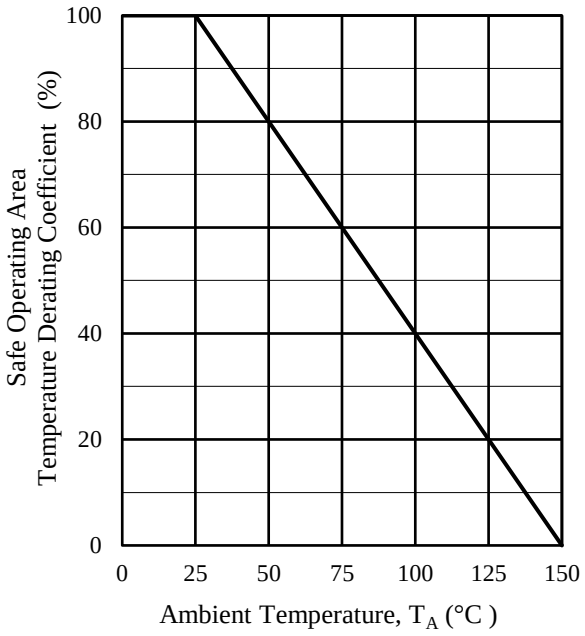


Figure 4-1. SOA Temperature Derating Coefficient Curve

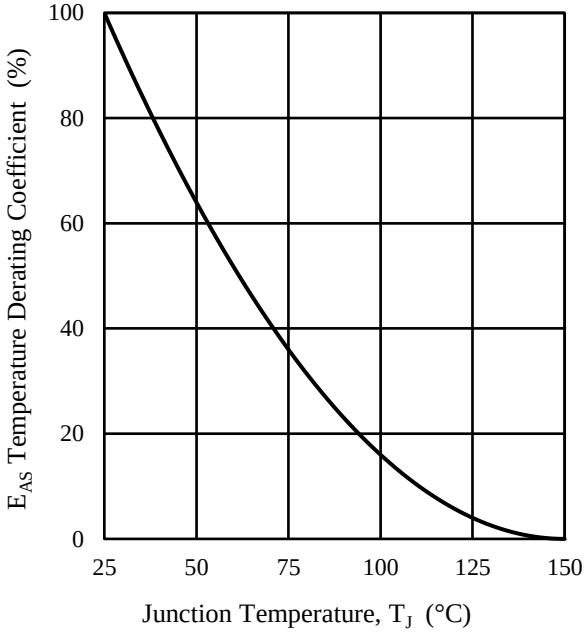


Figure 4-2. Avalanche Energy Derating Coefficient Curve

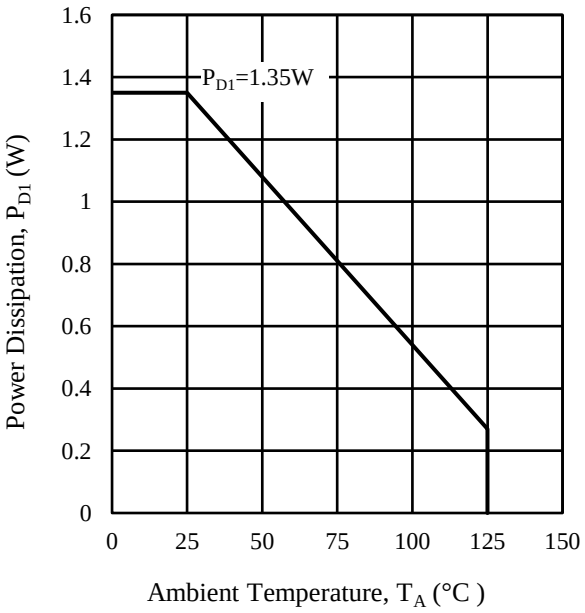


Figure 4-3. Ambient Temperature versus Power Dissipation Curve

4.2. MOSFET Safe Operating Area Curve

When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 4-1.

The broken line in the safe operating area curve is the drain current curve limited by on-resistance.

Unless otherwise specified, T_A = 25 °C and single pulse input.

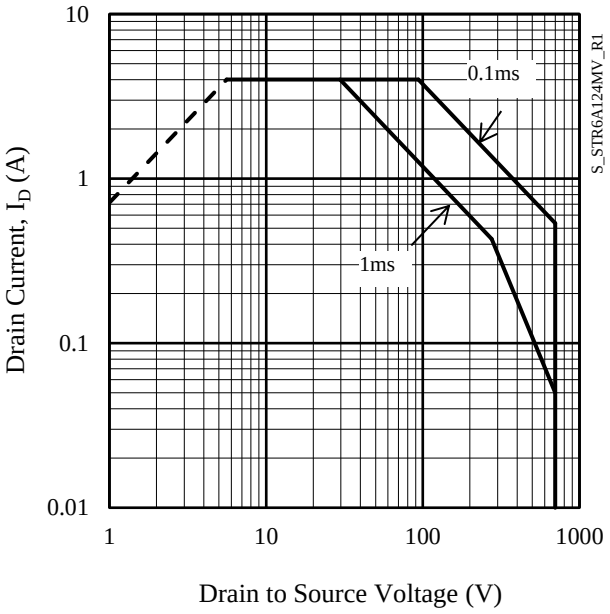


Figure 4-4. SOA Curve

4.3. Transient Thermal Resistance Curve

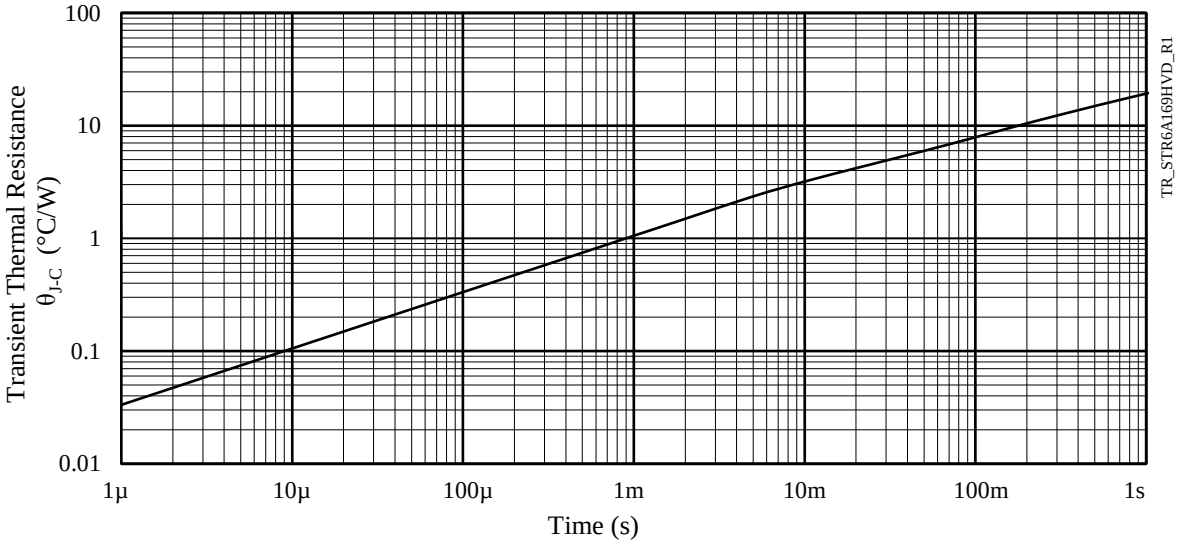
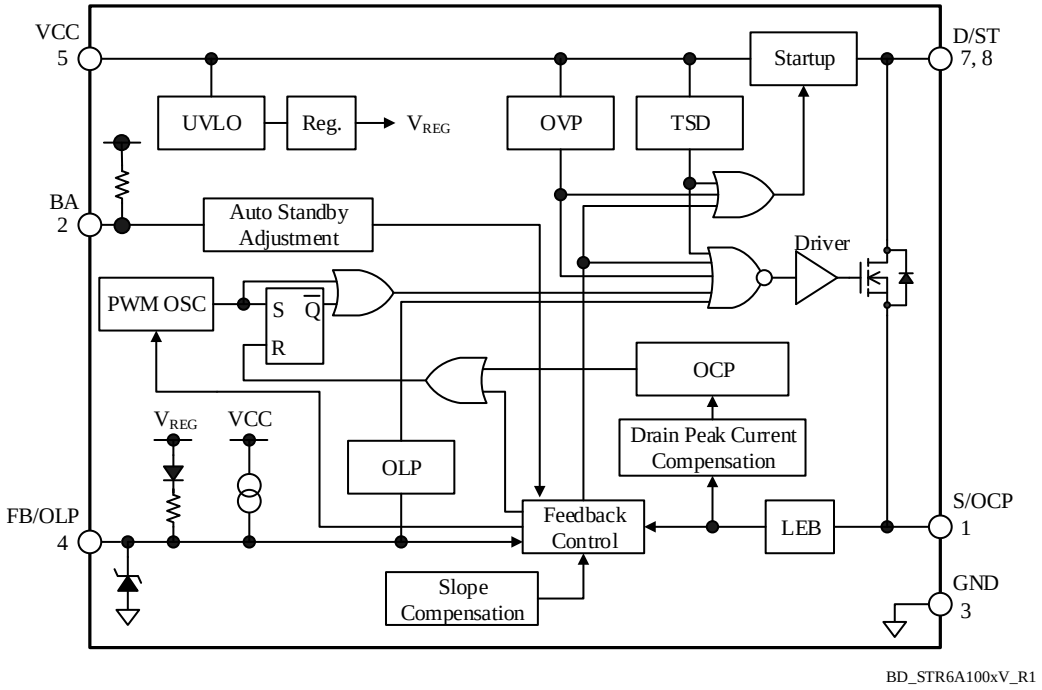
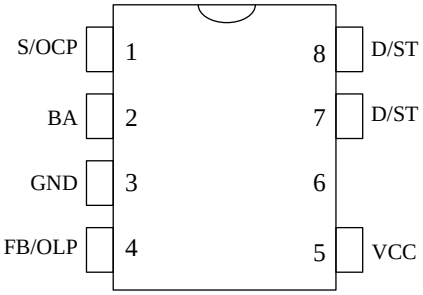


Figure 4-5. Transient Thermal Resistance Curve

5. Block Diagram



6. Pin Configuration Definitions



Pin	Name	Descriptions
1	S/OCP	MOSFET source and Overcurrent Protection (OCP) signal input
2	BA	Input of selectable standby operation point signal
3	GND	Ground
4	FB/OLP	Constant voltage control signal input and Overload Protection (OLP) signal input
5	VCC	Power supply voltage input for control part and Overvoltage Protection (OVP) signal input
6	–	(Pin removed)
7	D/ST	MOSFET drain and startup current input
8		

7. Typical Application

The PCB traces for D/ST pins should be as wide as possible, in order to improve thermal release capability.

In applications having a power supply specified such that D/ST pin has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

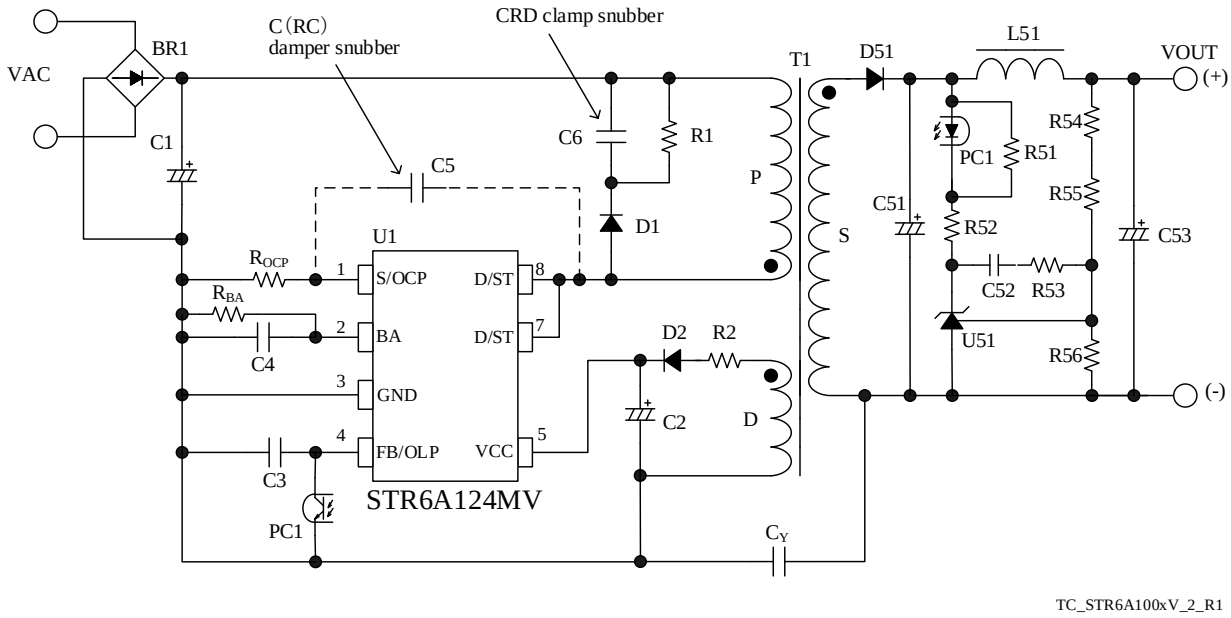
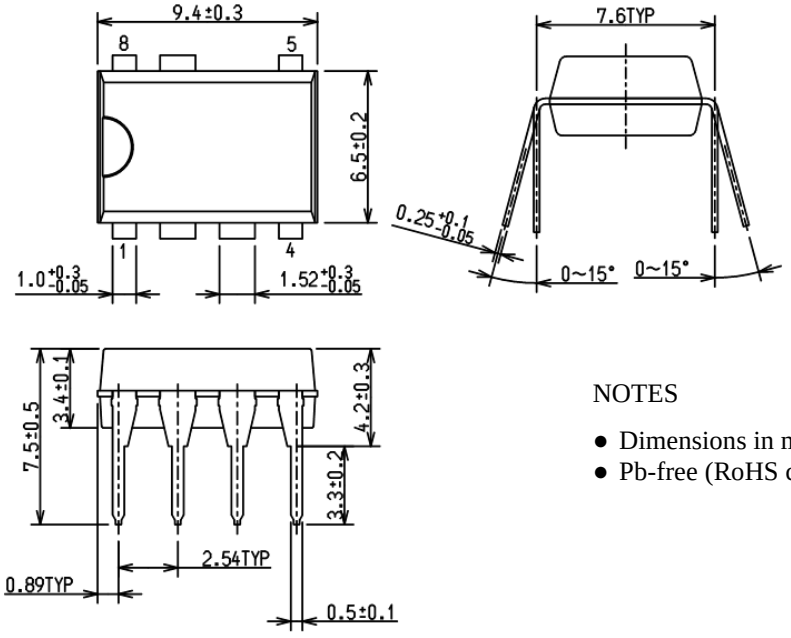


Figure 7-1. Typical Application

8. Physical Dimensions

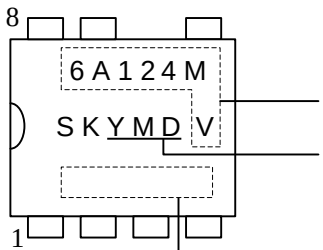
- DIP8



NOTES

- Dimensions in millimeters
- Pb-free (RoHS compliant)

9. Marking Diagram



Specific Device Code

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N or D)
D is a period of days,
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10-11 days of the month (21st to 31st)

Control Number

10. Operational Description

All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).

10.1. Startup Operation

Figure 10-1 shows the circuit around IC.

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{ST(ON)}$ = 47 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{CC(ST)}$ = −2.50 mA, charges C2 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts operation. During the IC operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 10-1 becomes a power source to the VCC pin. After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

$$V_{CC(BIAS)}(\text{max.}) < V_{CC} < V_{CC(OVP)}(\text{min.})$$

$$\Rightarrow\ 10.5\ (\text{V}) < V_{CC} < 27.0\ (\text{V}) \qquad (1)$$

The startup time of IC is determined by C2 capacitor value. The approximate startup time t_{START} (shown in Figure 10-2) is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{CC(ST)}|} \qquad (2)$$

where,

t_{START} is startup time of IC (s), and

$V_{CC(INT)}$ is initial voltage on VCC pin (V).

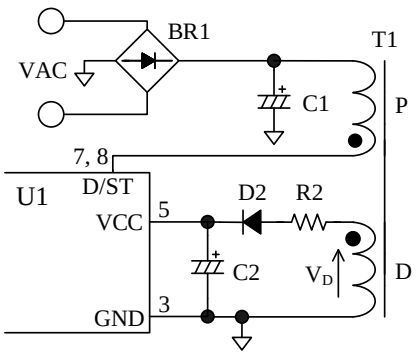


Figure 10-1. VCC Pin Peripheral Circuit

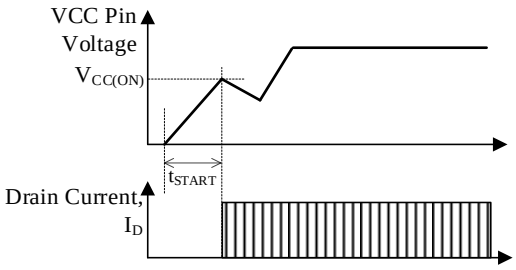


Figure 10-2. Startup Operation

10.2. Undervoltage Lockout (UVLO)

Figure 10-3 shows the relationship of VCC pin voltage and circuit current I_{CC}. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V, the control circuit stops operation by Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

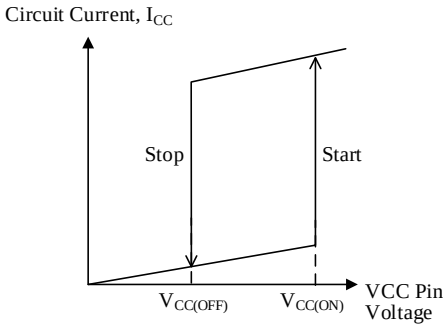


Figure 10-3. Relationship between VCC Pin Voltage and I_{CC}

10.3. Bias Assist Function

By the Bias Assist Function, the startup failure is prevented. The Bias Assist Function is activated, in both of following condition:

the FB pin voltage is FB/OLP Pin Oscillation Stop Threshold Voltage, $V_{FB(OFF)}$ or less

and the VCC voltage decreases to the Startup Current Biasing Threshold Voltage, $V_{CC(BIAS)}$ = 9.6 V.

When the Bias Assist Function is activated, the VCC pin voltage is kept almost constant voltage, $V_{CC(BIAS)}$ by providing the startup current, $I_{CC(ST)}$, from the startup circuit. Thus, the VCC pin voltage is kept more than $V_{CC(OFF)}$.

Since the startup failure is prevented by the Bias Assist Function, the value of C2 connected to VCC pin can be small. Thus, the startup time and the response time of the OVP become shorter.

The operation of the Bias Assist Function in startup is as follows. It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

Figure 10-4 shows VCC pin voltage behavior during the startup period.

After VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V at startup, the IC starts the operation. Then circuit current increases and VCC pin voltage decreases. At the same time, the auxiliary winding voltage V_D increases in proportion to output voltage. These are all balanced to produce VCC pin voltage.

When VCC pin voltage is decrease to $V_{CC(OFF)}$ = 8.5 V in startup operation, the IC stops switching operation and a startup failure occurs.

When the output load is light at startup, the output voltage may become more than the target voltage due to the delay of feedback circuit. In this case, the FB pin voltage is decreased by the feedback control. When the FB pin voltage decreases to $V_{FB(OFF)}$ or less, the IC stops switching operation and VCC pin voltage decreases. When VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist Function is activated and the startup failure is prevented.

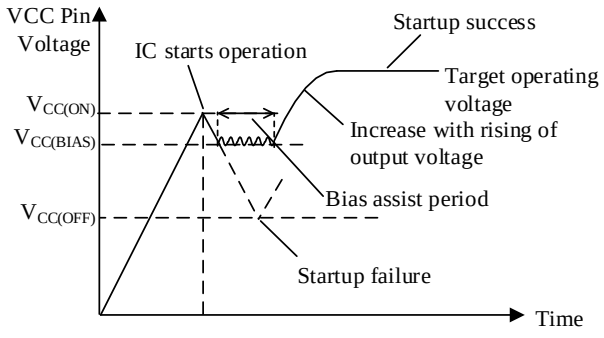


Figure 10-4. VCC Pin Voltage during Startup Period

10.4. Soft Start Function

Figure 10-5 shows the behavior of VCC pin voltage and drain current during the startup period.

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 8.75 ms. during the soft start period, over current threshold is increased step-wisely (7 steps). This function reduces the voltage and the current stress of MOSFET and secondary side rectifier diode.

Since the Leading Edge Blanking Function (see Section 10.6) is deactivated during the soft start period, there is the case that ON time is less than the leading edge blanking time, t_{BW} = 330 ns.

After the soft start period, D/ST pin current, I_D, is limited by the Overcurrent Protection (OCP), until the output voltage increases to the target operating voltage. This period is given as t_{LIM}.

In case t_{LIM} is longer than the OLP Delay Time, t_{OLP}, the output power is limited by the Overload Protection (OLP).

Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the t_{LIM} is less than t_{OLP} = 55 ms (min.).

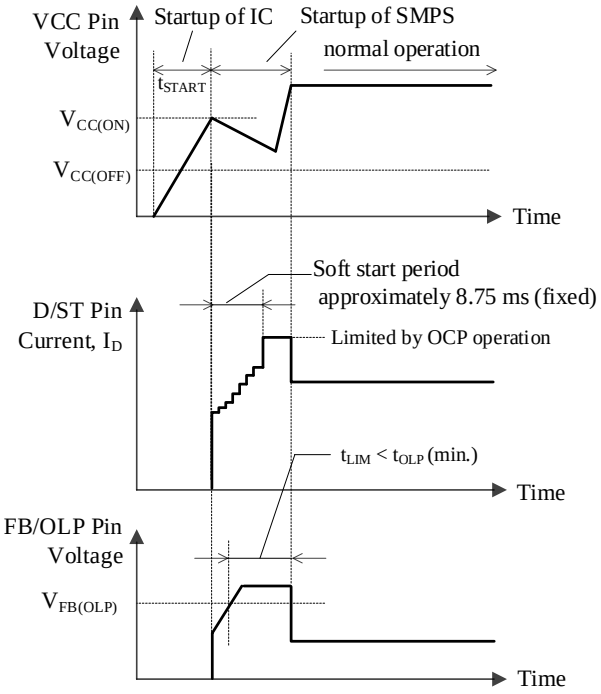


Figure 10-5. V_{CC} and I_D Waveforms during Startup

10.5. Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (see Section 5), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure 10-6 and Figure 10-7.

- Light Load Conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.

This control prevents the output voltage from increasing.

- Heavy Load Conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

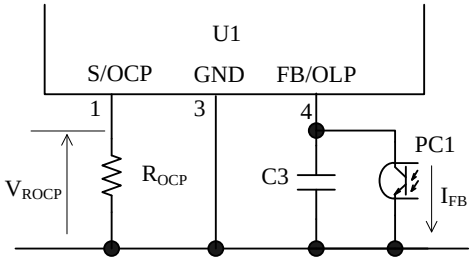


Figure 10-6. FB/OLP Pin Peripheral Circuit

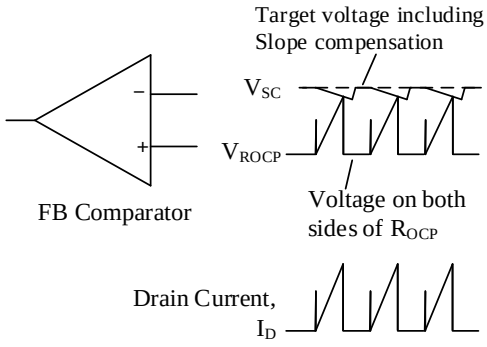


Figure 10-7. Drain Current, I_D, and FB Comparator Operation in Steady Operation

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 10-8. This is called the subharmonics phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation Function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the duty cycle gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

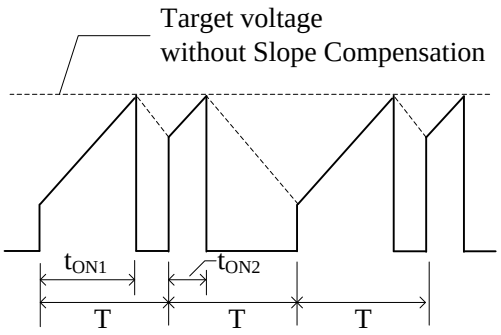


Figure 10-8. Drain Current, I_D, Waveform in Subharmonic Oscillation

10.6. Leading Edge Blanking Function

The constant voltage control of output of the IC uses the peak-current-mode control method.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of FB comparator or Overcurrent Protection circuit (OCP) to the steep surge current in turning on a power MOSFET.

In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking, t_{BW} = 330 ns is built-in. During t_{BW}, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V which is higher than the normal OCP threshold voltage (see Section 10.10).

10.7. Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

10.8. Step Drive Control

Figure 10-9 shows a flyback control circuit. The both end of secondary rectification diode (D51) is generated surge voltage when a power MOSFET turns on. Thus, V_{RM} of D51 should be set in consideration of the surge.

The IC optimally controls the gate drive of the internal power MOSFET (Step drive control) depending on the load condition. The step drive control reduces the surge voltage of D51 when the power MOSFET turns on (see Figure 10-10). Since V_{RM} of D51 can be set to lower value than usual, the price reduction and the increasing circuit efficiency are achieved by using a diode of low V_F.

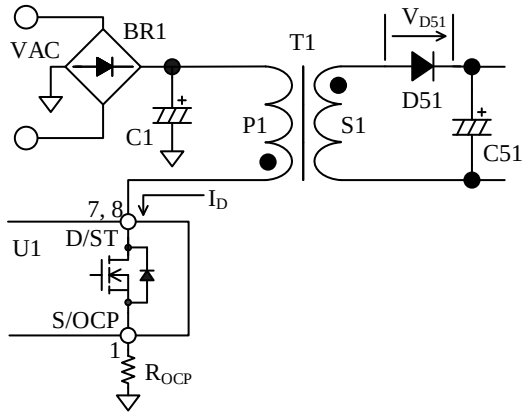


Figure 10-9. Flyback Control Circuit

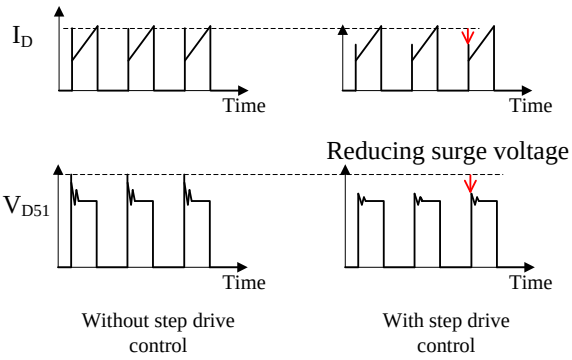


Figure 10-10. I_D and V_{D51} Waveforms

10.9. Operation Mode

The operation of the IC automatically changes to green mode or burst oscillation mode in order to reduce the switching loss (see Figure 10-11).

When the output load becomes lower, FB/OLP pin voltage decreases. When FB/OLP pin voltage decreases to $V_{FB(FDS)}$ or less, the green mode is activated and the oscillation frequency starts decreasing. When FB/OLP pin voltage becomes $V_{FB(FDE)}$, the oscillation frequency stops decreasing (see Table 10-1). At this point, the oscillation frequency becomes $f_{OSC(MIN)}$ = 25 kHz.

When FB/OLP pin voltage further decreases and becomes the standby operation point, the burst oscillation mode is activated. As shown in Figure 10-12, the burst oscillation mode consists of switching period and non-switching period. The oscillation frequency during switching period is the Minimum Frequency, $f_{OSC(MIN)}$ = 25 kHz.

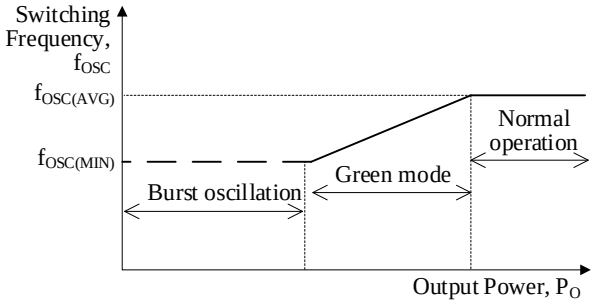


Figure 10-11. Relationship between P_O and f_{OSC}

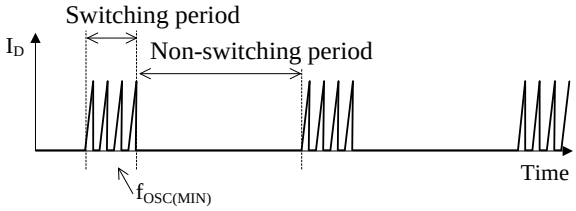


Figure 10-12. Switching Waveform at Burst Oscillation

Table 10-1. FB/OLP Pin Starting and Ending Voltage of Frequency Decreasing

	STR6A124MV (f_{OSC} = 65 kHz)
$V_{FB(FDS)}$ (typ.)	3.30 V
$V_{FB(FDE)}$ (typ.)	3.00 V

The standby operation point can be adjusted by the external resistor, R_{BA} (see Figure 10-13) according to the power supply specification.

Table 10-2 shows the load ratio of the standby operation point, where the load ratio at the Overcurrent Protection operating point is 100 %.

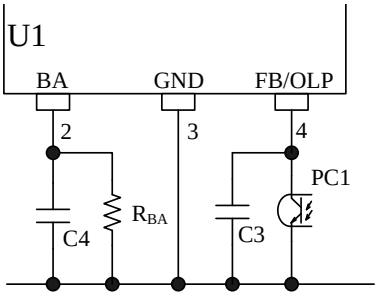


Figure 10-13. BA Pin Peripheral Circuit

Table 10-2. Standby Operation Point

R_{BA}	FB/OLP Pin Oscillation Stop Threshold Voltage STR6A124MV (f_{OSC}=65 kHz)	Output Power Ratio of the Standby Operation Point
Short	1.28 V	About 3 to 6 %
Open	1.63 V	About 4 to 8 %
330 kΩ	1.92 V	About 6 to 11 %
68 kΩ	2.17 V	About 8 to 13 %

Generally, to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst mode, audible noises can be reduced.

The OCP detection usually has some detection delay time. The higher the AC input voltage is, the steeper the slope of I_D is. Thus, the peak drain current at the burst oscillation mode becomes high at a high AC input voltage.

It is necessary to consider that the burst frequency becomes low at a high AC input.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.6 V during the transition to the burst mode, the Bias Assist function is activated and stabilizes the standby mode, because the Startup Current, $I_{CC(ST)}$, is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$. However, if the Bias Assist Function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary-side winding and/or reducing the value of R2 (see Section 11.1).

10.10.Overcurrent Protection (OCP)

10.10.1. OCP Operation

Overcurrent Protection (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage.

During Leading Edge Blanking Time, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V which is higher than the normal OCP threshold voltage as shown in Figure 10-14. Changing to this threshold voltage prevents the IC from responding to the surge voltage in turning-on the power MOSFET. This function operates as protection at the condition such as output windings shorted or unusual withstand voltage of secondary-side rectifier diodes.

When power MOSFET turns on, the surge voltage width of S/OCP pin should be less than t_{BW}, as shown in Figure 10-14. In order to prevent surge voltage, pay extra attention to R_{OCP} trace layout (see Section 11.2).

In addition, if a C (RC) damper snubber of Figure 10-15 is used, reduce the capacitor value of damper snubber.

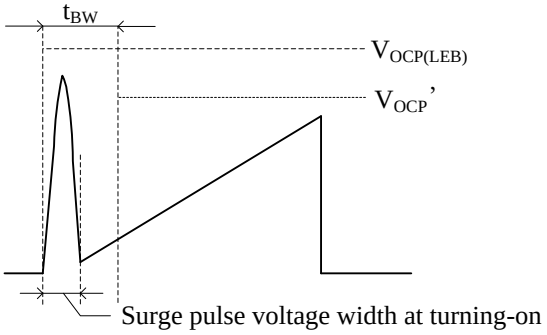


Figure 10-14. S/OCP Pin Voltage

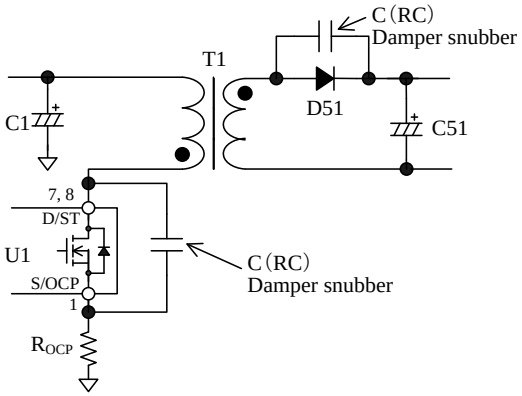


Figure 10-15. Damper Snubber

10.10.2. OCP Input Compensation Function

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to V_{OCP}. Thus, the peak current has some variation depending on the AC input voltage in OCP state.

In order to reduce the variation of peak current in OCP state, the IC incorporates a built-in Input Compensation Function.

The Input Compensation Function is the function of correction of OCP threshold voltage depending with AC input voltage, as shown in Figure 10-16.

When AC input voltage is low (duty cycle is broad), the OCP threshold voltage is controlled to become high. The difference of peak drain current become small

compared with the case where the AC input voltage is high (duty cycle is narrow).

The compensation signal depends on duty cycle. The relation between the duty cycle and the OCP threshold voltage after compensation V_{OCP}' is expressed as Equation (3). When duty cycle is broader than 36 %, the V_{OCP}' becomes a constant value $V_{OCP(H)}$ = 0.888 V

$$V_{OCP}' = V_{OCP(L)} + DPC \times ONTime$$

$$= V_{OCP(L)} + DPC \times \frac{Duty}{f_{OSC(AVG)}} \quad (3)$$

where,

$V_{OCP(L)}$ is OCP Threshold Voltage at Zero Duty Cycle (V),

DPC is OCP Compensation Coefficient (mV/µs),

ONTime is on-time of power MOSFET (µs),

Duty is duty cycle of power MOSFET (%), and

$f_{OSC(AVG)}$ is Average PWM Switching Frequency (kHz).

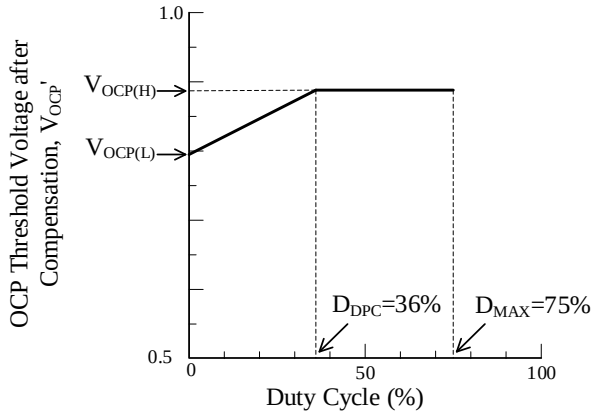


Figure 10-16. Relationship between Duty Cycle and Drain Current Limit after Compensation

10.11.Overload Protection (OLP)

Figure 10-17 shows the FB/OLP pin peripheral circuit, and Figure 10-18 shows each waveform for OLP operation.

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin and the FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 7.3 V or more for the OLP delay time, t_{OLP} = 75 ms or more, the OLP is activated, the IC stops switching operation.

During OLP operation, the intermittent operation by VCC pin voltage repeats and reduces the stress of parts such as the power MOSFET and secondary side rectifier diode.

When the OLP is activated, the IC stops switching operation, and the VCC pin voltage decreases.

During OLP operation, the Bias Assist Function is disabled. When the VCC pin voltage decreases to $V_{CC(OFF)SKP}$ (about 9 V), the startup current flows, and the VCC pin voltage increases. When the VCC pin voltage increases to $V_{CC(ON)}$, the IC starts operation, and the circuit current increases. After that, the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V, the control circuit stops operation.

Skipping the UVLO operation of $V_{CC(OFF)}$ (see Section 10.2), the intermittent operation makes the non-switching interval longer and restricts the temperature rise of the power MOSFET.

When the abnormal condition is removed, the IC returns to normal operation automatically.

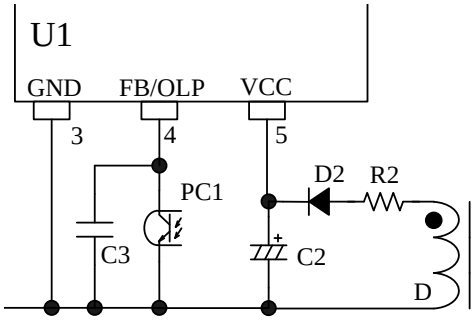


Figure 10-17. FB/OLP Pin Peripheral Circuit

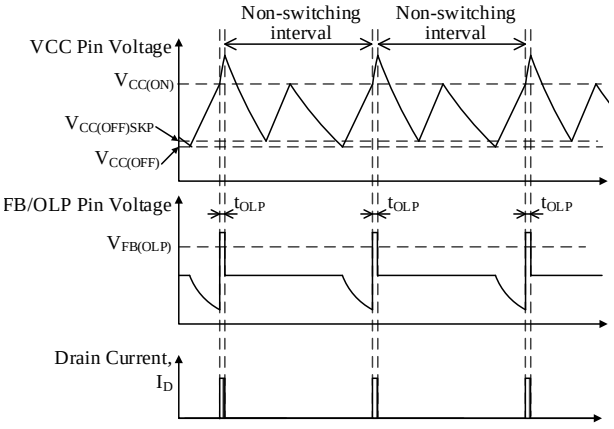


Figure 10-18. OLP Operational Waveforms

10.12.Overvoltage Protection (OVP)

When a voltage between VCC pin and GND terminal increases to $V_{CC(OVP)}$ = 29.1 V or more, Overvoltage Protection (OVP) is activated.

In case the VCC pin voltage is provided by using auxiliary winding of transformer, the overvoltage conditions such as output voltage detection circuit open can be detected because the VCC pin voltage is proportional to output voltage. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (4).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.1\ (V) \quad (4)$$

where,
$V_{OUT(NORMAL)}$ is output voltage in normal operation, and
$V_{CC(NORMAL)}$ is VCC pin voltage in normal operation.

When the OVP is activated, the IC stops switching operation at the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist Function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.

Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

10.13.Thermal Shutdown (TSD)

When the temperature of control circuit increases to $T_{J(TSD)}$ = 145 °C or more, Thermal Shutdown (TSD) is activated.

When the TSD is activated, the IC stops switching operation at the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist Function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$. Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

11. Design Notes

11.1. External Components

Take care to use properly rated, including derating as necessary and proper type of components.

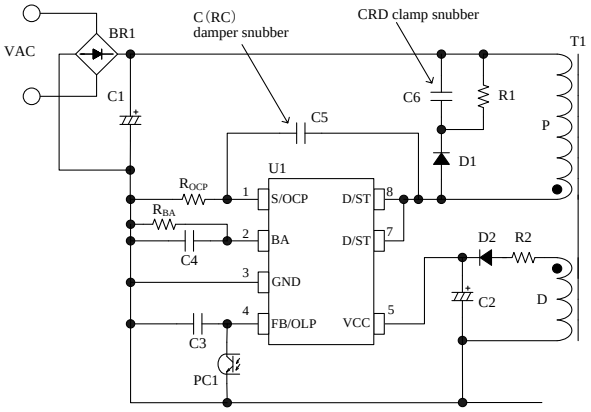


Figure 11-1. IC Peripheral Circuit

11.1.1. Input and Output Electrolytic Capacitor

Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

11.1.2. S/OCP Pin Peripheral Circuit

In Figure 11-1, R_{OCP} is the resistor for the current detection. A high frequency switching current flows to ROCP, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

11.1.3. BA Pin Peripheral Circuit

The FB/OLP pin oscillation stop threshold voltage is selected by the value of R_{BA} connected to the BA pin (see Section 10.9).
The reference value of C4 is from 1000 pF to 2200 pF for high frequency noise rejection

11.1.4. FB/OLP Pin Peripheral Circuit

C3 is for high frequency noise reduction and phase compensation, and should be connected close to these pins. The value of C3 is recommended to be about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

11.1.5. VCC Pin Peripheral Circuit

The value of C2 is generally recommended to be 10 µF to 47 µF (see Section 10.1, because the startup time is determined by the value of C2).

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 11-2), and the Overvoltage Protection (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 11-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

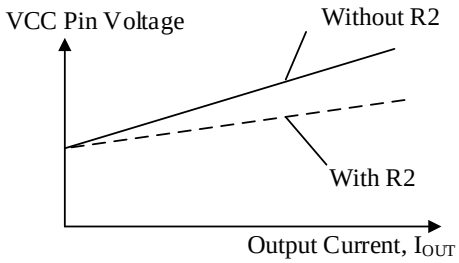


Figure 11-2. Variation of VCC Pin Voltage and Power

11.1.6. Snubber Circuit

In case the surge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 11-1);

- A clamp snubber circuit of a capacitor-resistor- diode (CRD) combination should be added on the primary winding P.
- A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/GND pin.
  In case the damper snubber circuit is added, this components should be connected near D/ST pin and S/OCP pin.

11.1.7. Phase Compensation

A typical phase compensation circuit with a secondary shunt regulator (U51) is shown in Figure 11-3.
C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047µF to 0.47µF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

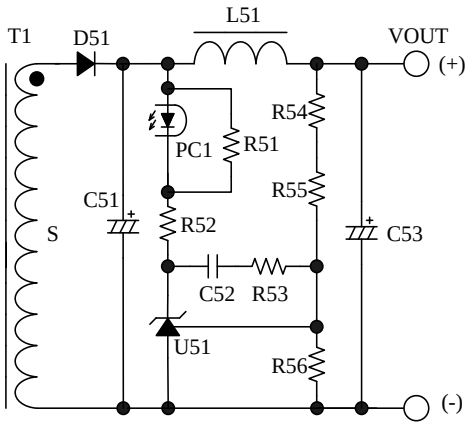


Figure 11-3. Peripheral Circuit Around Secondary Shunt Regulator (U51)

11.1.8. Transformer

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.

If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

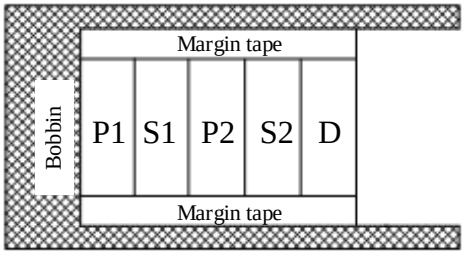
When the surge voltage of winding D is high, the VCC pin voltage increases and the Overvoltage Protection (OVP) may be activated. In transformer design, the following should be considered;

- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

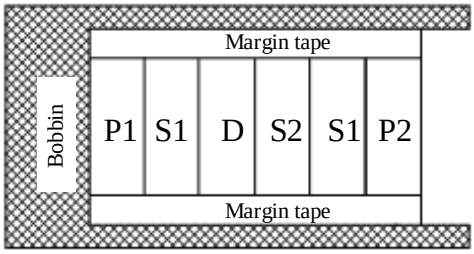
In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and

the others (S2, S3···) should be maximized to improve the line-regulation of those outputs.

Figure 11-4 shows the winding structural examples of two outputs.



Winding Structural Example (a)



Winding Structural Example (b)

Figure 11-4. Winding Structural Examples

- Winding Structural Example (a):
  S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2.
  D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

- Winding Structural Example (b)
  P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.
  D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.

11.2. PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 11-5 shows the circuit design example.

(1) Main Circuit Trace Layout
This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.
If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout
Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 11-5 as close to the R_{OCP} pin as possible.

(3) VCC Trace Layout:
This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the GND pin is recommended.

(4) R_{OCP} Trace Layout
R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 11-5) which is close to the base of R_{OCP}.

(5) Peripheral components of the IC
The components for control connected to the IC should be placed as close as possible to the IC, and should be connected as short as possible to the each pin.

(6) Secondary Rectifier Smoothing Circuit Trace Layout:
This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations
Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.
Since the copper area under the IC and the D/ST pin trace act as a heatsink, its traces should be as wide as possible.

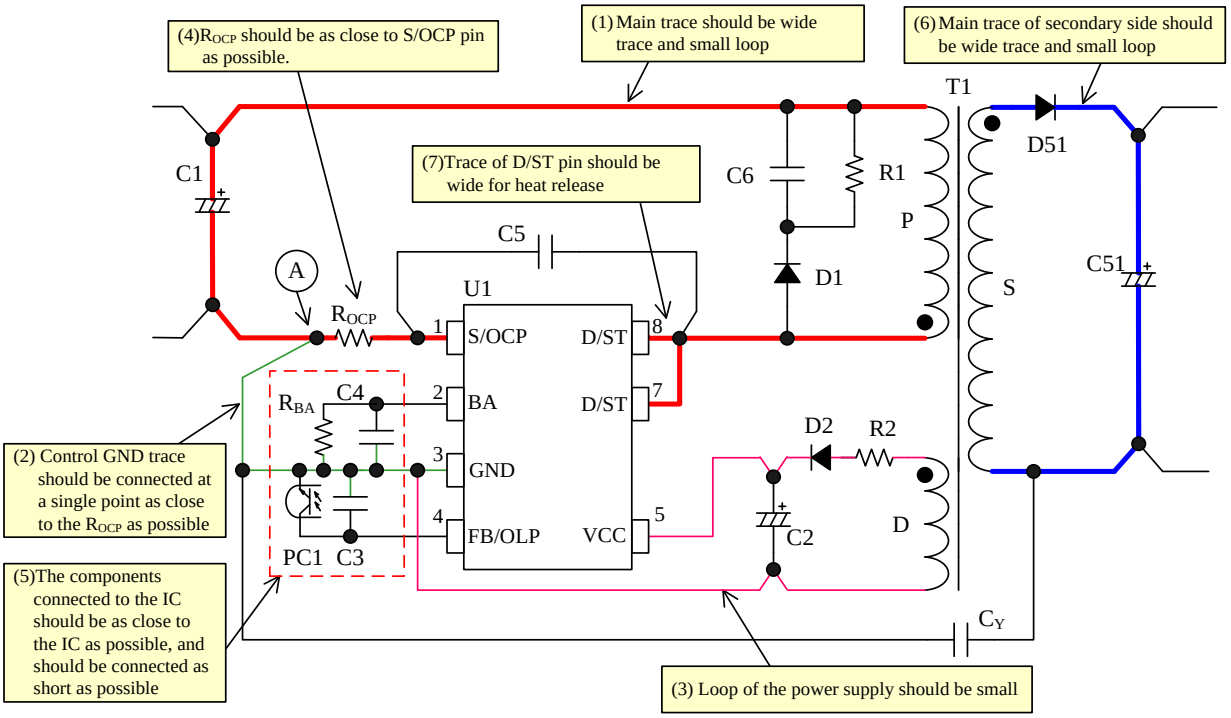


Figure 11-5. Peripheral Circuit Example Around IC

12. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of circuit using STR6A124MV. The PCB pattern layout example is made usable to other ICs in common. The parts in Figure 12-2 are only used.

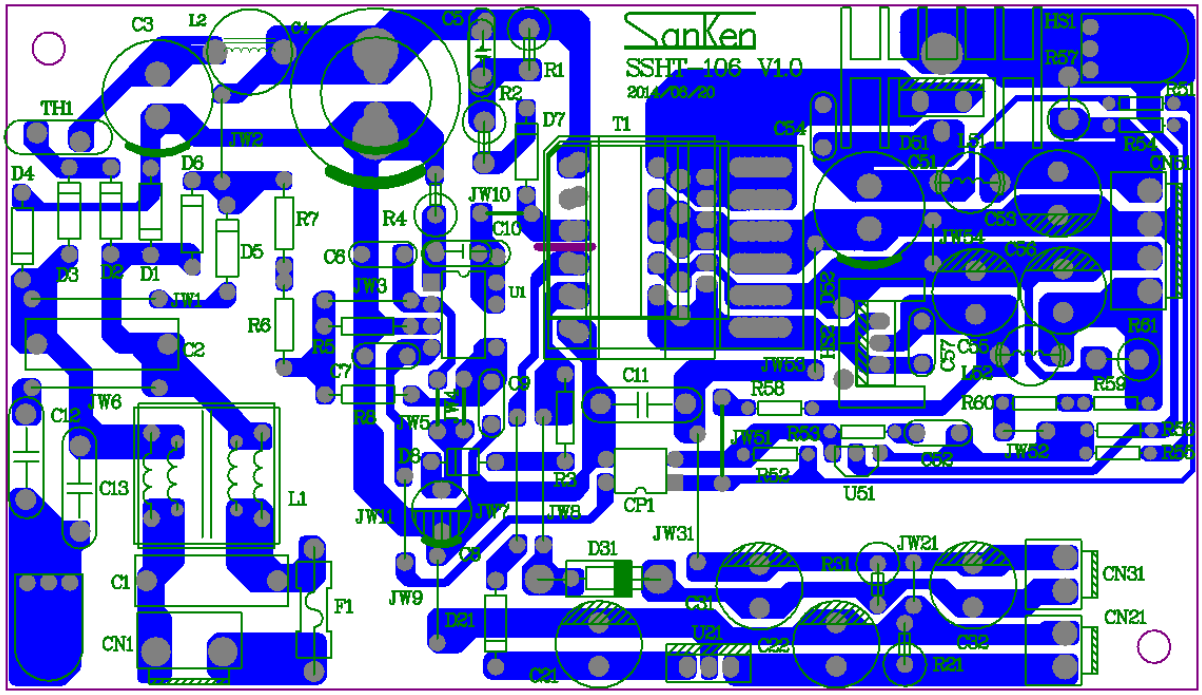


Figure 12-1 PCB Circuit Layout Example

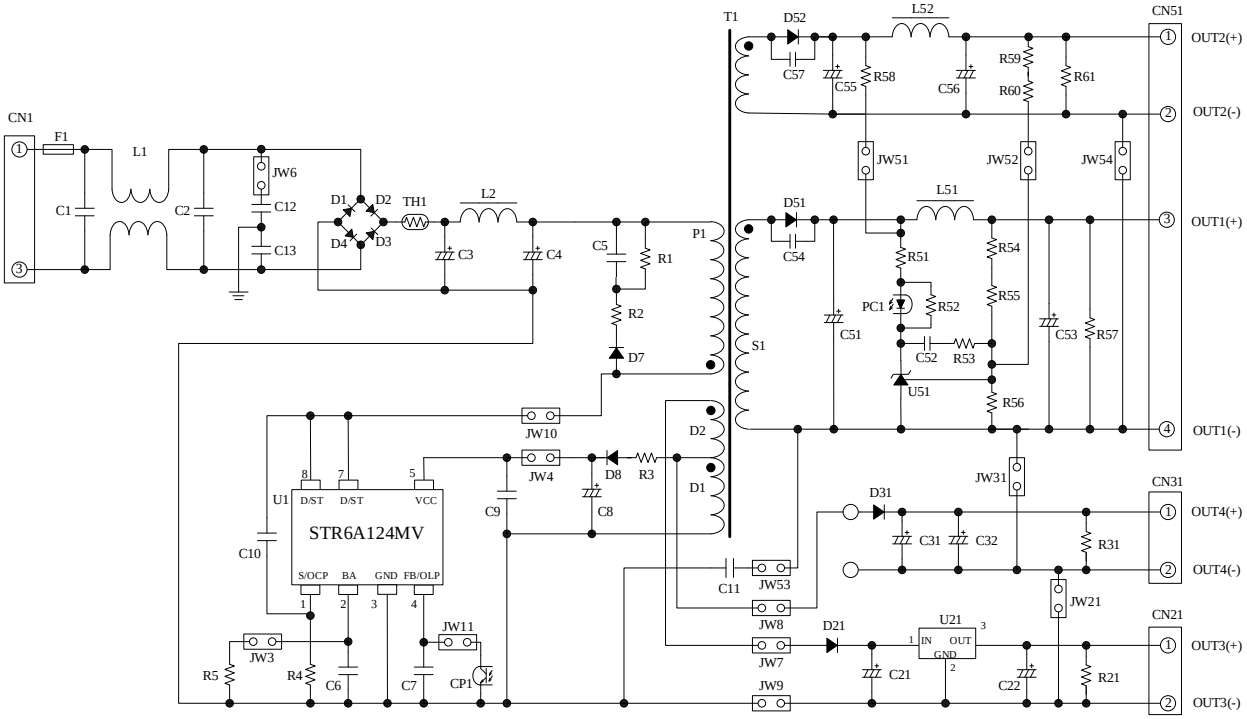


Figure 12-2 Circuit Schematic for PCB Circuit Layout

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